Next Generation Memory Interfaces

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Acknowledgement

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Integrated Circuit

Next Generation Memory Interfaces

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Abstract

As DDR memory technology has increased its pace transferring from DDR3 to DDR4, the design of the physical layer complying DDR4 JEDEC has become essential to memory controller overall performance. This work presents the design of the transmitter block implementation inside the physical layer of the memory controller running with 3.2GHz. Detailed design have been analyzed for implementing the transmitter which is able to provide adjustable matched impedance with transmission line and meanwhile having the output swing complying the DDR4 JEDEC specification. Two impedance line models was used in the simulation. This work also conducts a comprehensive research of the current DDR4 technology in the aspect of industry trend, potential market size, potential customers, competitive technologies and intellectual property issues.

Next-Generation Memory Interfaces Capstone Report

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Project Context and Introduction

As a team we designed and tested the physical interface (PHY) for DDR4 memory. Our PHY design is to be used by the Berkeley Wireless Research Center (BWRC) in future research projects. The PHY is an essential circuit block that facilitates the communication between a memory controller and the DDR4 memory itself. Figure 1 illustrates where the PHY exists in a typical computer's data flow.
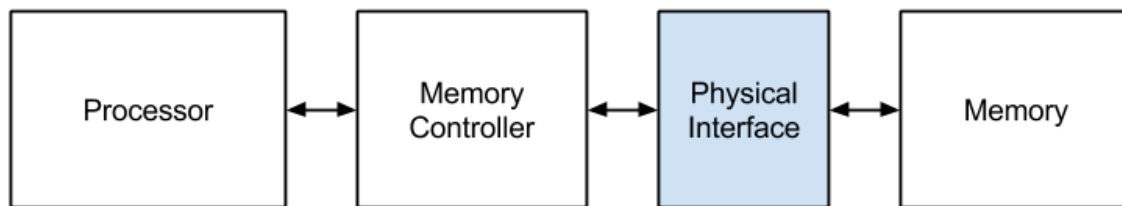
Figure 1. Simplified flow diagram of data between the processor and memory in a typical computer system.

DDR4 is the latest generation of high-speed Dynamic Random Access Memory (DRAM). DRAM is used widely in nearly every modern computer system including laptops, desktops, smartphones, and servers. DDR4 is faster and more energy efficient than it's predecessors, and it's crucial that BWRC leverage this technology in their research. Our PHY block is an integral part in enabling the use of DDR4.

The PHY has been divided into five separate circuit blocks, two digital blocks and three analog blocks. The digital blocks have been designed and verified through place and route. The analog blocks have been modeled in VerilogA and circuits have been designed that fit these models. Furthermore, we designed the circuits using an educational 32nm/28nm technology. As such, we have not designed the PHY to tape-out and it will not

be manufactured. However, the IP (Verilog source code and circuits) are provided to BWRC so that they are able to develop the circuits in a usable technology if desired.

We've integrated all blocks into Cadance as individual circuit blocks and wrapped them in a top-level test infrastructure to verify that all blocks communicate properly with one another. For more information regarding the different circuit blocks, see the Technical Contribution section of this paper.

This paper consists of an industry and market analysis for the semiconductor/memory industry, an IP strategy including the possibility for a patent, and my personal technical contributions to the project.

Industry, Market and Trends Analysis

In this section we will investigate the current semiconductor industry, what technologies exist and how our technology fits, and elaborate on the current competitive landscape of the market. We will also establish our possible clients, stakeholders, and our go-to-market strategy. Finally, we will evaluate the current social, technological, and economic trends and how these forces affect the industry.

Integrated circuits are an important sector in the semiconductor industry. The semiconductor industry is known to be highly competitive in nature, and the trend has been increasing over the years (Ulama 2014:19). Product life cycles are short, as more technologically advanced products replace older ones. Adoption of products is majorly affected by performance and reliability. The notable companies in the integrated circuits industry are Intel Corporation and Samsung Electronics with 7.6% and 5.3% of the global semiconductor and electronics parts manufacturing market, respectively (IBISWorld 2015:

27). Broadcom Corporation, Texas Instruments Inc., Advanced Micro Devices (AMD) Inc., Micron Technology Inc. are a few of the other major companies that compete in this industry (Ulama 2014:19). The major companies in this industry are all fairly large and well established, and compete over products and technologies. High demand for products and extremely low pricing intensify the competition in the industry. This poses a significant barrier to entry for new and smaller companies leading to only several companies currently building DDR4 memory chips and controllers. In fact, Micron and Samsung is the only one of the large integrated circuits companies listed above that develops DRAM technology.

As we strive to make a smaller, faster, and more efficient memory interface, we have to compete with the products, research and development efforts of competing companies. Our competitive landscape does not merely include semiconductor companies, but also technologies that have similar features and functions when compared against our project. Existing memory technologies, such as DDR3, 3D stacked (3DS) - DDR3, and GDDR4, compete with DDR4 on various parameters such as cost, speed, and use-cases. While DDR4 is faster than previous memory generations, the higher cost of the new chip technology would make the cheaper DDR3 technology a strong competitor.

Emphasis is placed on the significant performance improvements that DDR4 presents over DDR3 technology. The following table shows a brief comparison of the key features between two technologies.

Table1. Comparison between DDR3 and DDR4 [1]:

	DDR3	DDR4
Power supply voltage	1.5V	1.2 V

Speed	1.6~2.1 Gbps	1.6~3.2 Gbps
Density	8GB(max)	16GB(max)
Price	$100 avg	$200 avg.

The first comparison is in regards to power efficiency, not only does DDR4 have a lower supply voltage, but it also implements a new algorithm to control its energy consumption by entering its "standby" mode more frequently and precisely than DDR3. The improvements lead to better performance in both the power consumption, and operating temperature.

Furthermore, the most essential feature, memory speed, has been improved significantly in DDR4. The analogy between the memory speed and highway traffic speed is very descriptive. The speed of the memory is the amount of data can be transferred in a certain period of time. There are two factors determining the speed, which are, interface width and frequency of the memory's operation. Considering the analogy, the bandwidth is the quantity of lanes on a highway, and frequency is the travel speed of its vehicles. Within a fixed time period, having more lines and a faster speeds will allow for more vehicles to travel. Similarly, having an improved working frequency, along with an enlarged bandwidth, DDR4 achieves a data transmission speed that is approximately 1.5 times faster than DDR3, as Table 1 indicates. The increase of the speed is benefited from the revolutionary bank-group management technology.

Another differentiating factor is the density, or say, the space of a single memory chip. Advancements in the chip's encapsulation provide DDR4 a 50% density increase, with regard to maximum space. With a larger storage space, DDR4 is able to process more information simultaneously. However, similar to every emerging new technology, the

current price of DDR4 memory is 30% to 50% more expensive than DDR3, which can achieve similar functionality at lower speeds. With a large-scale adaptation for DDR4 memory, and hardware compatibility of its peripheral devices, the manufacture price would quickly become more affordable in the future.

GDDR3 and GDDR5, which stand for Graphics Double Data Rate, are a kind of memory specifically designed for image processing. Despite the similarity in terms of the name, the graphic memory is named one generation ahead regular memory. This means that the core technology of GDDR3 is essentially an upgraded version based on DDR2 technology, rather than DDR3. The graphic memory is designed to have lower energy consumption, and an optimized performance when dealing with graphical-data processing. Since the application area of these two kinds memory differentiates amongst each other, they do not compete directly. The Graphic DDR is typically developed based on the previous generation of DDR memory technology, with improvements on speed aand application-specific functional modifications.

As for the market analysis of our product, the main markets include traditional memory devices and consumer electronics - and they are booming. Based on transparency market research, it states that the global next generation memory technologies market was worth $207.8 million in 2012, and is projected to be worth $2,837.0 million by 2019, growing at a 46.1% average growth rate from 2013 to 2019 (Transparency Market Research, 2014). The report divides the overall market for next generation memory technologies on the basis of certain parameters: interface type, application, and geography. On the basis of interface, the market for next generation memory technologies can be categorized into SATA, SAS, DDR, and PCIe and I2C (Transparency Market Research,

2014). The main applications of next generation memory technologies include embedded MCU and smart card, mobile phones, mass storage, cache memory, enterprise storage, and automotive.

Geographically, the global next generation memory technologies' markets can be divided into North America, Europe, Asia-Pacific, and the rest of the world. This industry is always looking for ways to decrease power consumption, increase density, and develop clever architectures. The new generation memory technologies market has gained significant momentum in recent years due to growing demand for faster, highly scalable, and cost-effective memory solutions.

Understanding the necessity of our effort follows from understanding the industry dynamic, which our product tempts to enter. After understanding the landscape within which we stand, we remain to have reason to believe that our project is valuable to our stakeholders. We remain to reason that our stakeholders should be more interested in receiving a completed deliverable from us over any other, equally qualified, external competitor.

Our first differentiating quality is that we offer to provide "non-contracted" work. Contracted work is any work commissioned by one party to be executed by another party. To begin such work, both parties must agree on the terms defined within the agreement document prior to the work's commencement. The agreement is realized through means of a binding contract that both parties agree to enact. Once the contract is created, it typically cannot be altered or modified, unless the consent of all parties is evident. This could place the requesting party into a stiff situation if it discovers that its priorities have changed mid-way through a contract.

Upon the project's completion, the completed work is commonly handed off "as-is." This means that no additional support is to be provided in the future (unless explicitly negotiated upon within the original contract). Any additional requested support or modification requires for a new contract to be written. Not only is this financially inconvenient, but it can also be logistically inconvenient for the recipient. Without support, the deliverable is handed off with a decreased utility. The recipient of the deliverable is stuck with using the deliverable solely within its original scope.

Our stakeholder, BWRC, benefits from ownership over the development process. A common clause added to most contractual work instills a limit on interim design modification requests. This clause exists to prevent the requesting party from overexerting the contracted party without compensation. Internal control over the developmental process allows for precise design-source malleability during development, and full exposure of the design files. Design-source malleability allows for the BWRC professors to more closely guide our direction through the project's development. It allows for them to change the path that we follow if new interests arise. There is no contractual overhead to worry about in this scenario.

BWRC benefits from retaining access, and owning, the source code and designs. The design-source exposure enables BWRC to question every aspect of the implementation until they understand it completely. With contracted work, this information is typically unavailable to the requesting party due to trade secrets being used in a design. Owning the source enables BWRC to have permanent design-source access. Long-term source access enables cost-effective and effort-effective technology adaptation into any future BWRC

projects. Along with adaptation, owning the source creates the opportunity for growing in-house expertise at BWRC through education.

The benefits mentioned above align very closely with our stakeholder's interests. The stakeholder, being BWRC, is interested in three main attributes from the project. First, BWRC wants a fully customizable deliverable due to unpredictable future demands. Second, BWRC wants the freedom to optimize the design for unique implementations that would require the modification of the source on a per-use basis. Third, BWRC wants to avoid the financial, temporal, and contractual overheads associated with third-party work. Our project delivers on all three attributes. By choosing to complete this project through our team, rather than a team of contractors, BWRC satisfies its internal interests.

Our team anticipates BWRC's decision to work with us as opposed to larger suppliers. The current semiconductor marketplace is saturated with both customers and suppliers. As Ulama describes (Ulama 2014:28), "Established operators in this industry have been able to develop solid relationships with customers, and it can be extremely difficult for new companies to gain contracts with customers when existing semiconductor manufacturing operators have built reputations over a long period." To exemplify the significance and the weight carried by the previous statement, note that the Semiconductor and Circuit Manufacturing industry is one of the largest exporting industries in the United States (Ulama 2014:5). It indirectly provides jobs to 250,000 Americans, is currently valued at $79.5 billion, and has grown at an annual rate of 4.8% (Ulama 2014:5).

The current players, both customers and producers, are very well established, and very tightly connected. Penetrating into the customer base that the massive producers currently support is near impossible for a small team like ours due to lack of reputation.

Aside from penetrating, the customers in this segment of the market are a significantly strong force due to two reasons: 1. The intrinsic competitiveness of the current suppliers, and 2. "The electronics marketplace is continually under pressure to improve product functionality, decrease size, increase speed, and decrease cost." (IBISWorld Global Semiconductor & Electronic Parts 2015:33)

Our team has set our target in a completely different direction. Instead of focusing on the massive customers, who are already served very competitively, we direct our focus at an interestingly under-served segment in this market space. In part, our choice of direction is due to the methods through which our Capstone project was decided upon. The decision process confined the scope of the project to target academic goals and provide solutions for academic institutions. Thus, our customer space currently only encompasses the Berkeley Wireless Research Center, but is functionally able to serve any academic or small-scale organizations.

As we currently stand, with one effective customer in our sights, we are subjecting ourselves to a very strong customer market force. This is an undesirable outcome due to the limited size of the space, which we choose to attack, but success in this space will send positive signals at other research institutions. We would be able to expand to encompass more academic institutions because they would prefer to acquire the product through us. Our effective results are comparable to their current methods of operation, but with the benefit of reduced fixed-cost expenditures – which arise when placing orders with large design and manufacture firms.

A majority of the market belongs to other companies, most all companies are well establish large corporations including Micron (IBISWorld 2015: 27) and Texas

Instruments (IBISWorld 2015: 30). The barriers that cause this include "access to latest technology and intellectual property, the level of investment…, access to skilled employees, and the dominance of existing players" (IBISWorld 2015: 25). In the memory industry, the companies compete over a very specific set of criteria including price, performance, features and power consumption, all of which are highly measurable and quantifiable metrics (IBISWorld 2015: 24).

If the dimensions of competition between companies in a given industry converge, then the companies are left to compete solely on price (Porter 2008: 12). In the integrated circuit market, the industry has converged heavily on these metrics of performance, features and power consumption, which has resulted in fierce price competition. Because "economies of scale can be significant in this industry" (IBISWorld 2015: 25), new entrants must manufacture large volumes to stand a chance against the bigger companies. This requires up-front capital that many smaller new entrants do not have available. Entering the market attempting to compete on these highly competitive dimensions would result in "zero sum competition" (Porter 2008: 13), and and would not be a viable business strategy.

When instead of converging on the same dimensions, companies target different segments of the customer base, the result can be "positive sum" competition: competition that increases the profitability of all companies (Porter 2008: 13). We plan to employ this strategy with our DDR4 memory controller. We've learned from BWRC that their needs are different than the typical semiconductor customer. BWRC fabricates chips in low volumes, so price is not a significant factor. Also, they require only a subset of the industry-standard feature set for DDR4 memory controllers, enabling us to reduce the size of the

design. Finally, they need very specific portions of the controller designed, not the entire IP block that most competitors would offer.

Although the memory technology industry is highly competitive, growing, and difficult to penetrate, the market is growing fast due to this a demand for consumer electronics, an industry which is expected to grow 5.3% annually to nearly $300 billion dollars by 2019 (IBISWorld 2014: 4). This high demand and new market bring some space for new companies to enter and grow. These new entrants usually emerge during the transition between the technological revolutions and each one has its own speciality.

From the year of 2002 to 2013, DDR memory industry has undergone 4 significant technological transitions, all of which are aiming at improving in three performance aspects and achieving a denser data processing capability. As Darryle stated in the article, the product with "high levels of performance, reliability, quality and low levels of power consumption" (Bach,2014:6) can gain an apparent advance in the competition of memory design industry. Being the three largest manufactures of memory chip and developer of DDR memory technology, Samsung, Crucial (Micron) and Hynix have already invested millions of dollars in their R&D sector to develop the new generation DDR4 memory interface in order to reinforce their dominating market share.

Given such a giant market, other major memory designers such as Kingston keep fastening their pace to catch up the memory controller design for the recent DDR3 to DDR4 transition. Besides the companies who are already in the market, there are significant number of new companies or say, new entrants, trying to seize this opportunity. According to the statement made by Darryle, "the latest Census data indicates that 64.1% of operators in this industry have fewer than 20 employees" (Ulama 2014:25). The development

strategy of those new entrants are highly focused on certain features, and "specializing in a small number of product lines to serve niche markets" (Ulama 2014:25) in order to avoid a direct competition with large companies.

Table 2. Representative new entrants in DDR4 memory development

Company Name	Specialized market/feature
Century Micro INC.	Small physical size & low energy consumption
Montage Technology	Fast operating speed & low energy consumption
G.SKILL	Enhanced gaming performance

Three unique, representative companies are provided to conduct the analysis of the new entrant. The table 1 above shows a brief comparison of three distinguished new entrants key product features. It indicates each new entrant is trying to gain its market share by specializing its product from the three technical aspects mentioned in the previous paragraph.

The Japanese based company Century has just halved the physical size of DDR4 memory in their most recent product at the year of 2014. The China-based Montage Tech is more focusing on developing fast speed and lower power rate DDR4 memory for large scale server use. "Less power draw means less heat and longer battery life", which indicates "the servers are expected to be the biggest beneficiaries of the jump to DDR4" (Andy, 2014:6). Meanwhile, G.SKILL put majority of its resources into developing DDR4 memory controller with improved gaming performance. These companies are increasingly securing their niche markets by making breakthroughs in design of the memory controller while the major developers are still dominating the memory chip manufacturing area.

Big companies enjoy economies of scale, making it difficult to compete with them in manufacturing the integrated circuits (ICs). Based on the analysis of the new entrants, in order to build immunity for our design, we plan to segment the market to research institutes like BWRC. Their needs are different from most, and provide an opportunity for us to develop a product that satisfies these needs better than the competition. Since the design of our project is specifically for BWRC internal research use, there will be no direct competition and obvious threat from these new entrants either.

The threat from other technologies is weaker, as our DDR4 interface is more advanced than existing DDR3/GDDR5 interfaces. Therefore, we focus on developing the intellectual property and targeting the specific needs of the academic communities. This specific category of consumers require more customizable, and open, circuit designs at a lower volume, a need that is unmet by the larger companies that package their circuits in black boxes, manufacture in high volume, and allow little to no customization. By segmenting the market based on unmet needs, and our abilities to satisfy them, we hope to entrench our position as a profitable part of the semiconductor industry.

From the perspective of semiconductor circuit design, it is a complicated process to design a controller and integrate it with the memory chip. Therefore, our technology suppliers include both software side and hardware suppliers. Software suppliers are those who provide coding languages, design platforms, and simulation tools. Hardware suppliers are those who provide electrical specifications, datasheets, and other fabrication characteristics relating to memory chips.

Software suppliers mainly provide programming language support. Verilog and SystemVerilog are the two main programming languages we are using. They are hardware

description languages used to model electronic systems. They are most commonly used in design and verification of digital circuits. Cadence, a company that provides electronic design automation software, covers many language design platforms, including Verilog and SystemVerilog. As an all-in-one suite, Cadence is our main software supplier.

Hardware suppliers provide descriptive information about the memory chip technology. Our controller is on a software level, but it will be integrated with the next generation memory chip technology, the DDR4 technology. Each generation of memory chips has new fabrication breakthrough. Thus, during our controller design, the latest information about memory chips is critical, such as voltage supply of the chips and the memory bank structure. Our hardware suppliers, such as Micron Technology, Intel Corp., and Samsung, are big semiconductor companies in this industry. In Semiconductor & Circuit Manufacturing in the US Industry Report, Intel Corp. and Samsung have 18% and 13.8% market share in 2014 (Ulama 2014:4). Although they seem like our competitors from the sales end, they also have the best research departments and technical experts in the chip fabrication domain. Samsung competes in the Semiconductor and Circuit Manufacturing industry via its fabrication and research and development facilities in the United States (Ulama 2014:4). They will release the paper and datasheet of their latest research results about DDR4 memory chip. According to the information provided by these large semiconductor-manufacturing companies, we are able to define the interface and design our memory controller.

Powerful suppliers capture more of the value for themselves by charging higher prices, limiting quality or services, or shifting costs to industry participants. As mentioned above, Intel Corp. and Samsung are both suppliers and competitors for us. If they limit our

access to their latest technology about DDR4 memory chip, it will be hard for us to compete with them. However, the good news is that the DDR4 memory specification is becoming a standard, so we will be less dependent on them.

There are certain aspects that we can focus on to succeed in this capital-intensive, and research-intensive, memory design industry. New companies are trying to explore the market by boosting their expertise in faster-speed designs, smaller dimension layouts, and highly customized application-specific designs. WIth increasing maturity of the DDR4 technology, the competition is becoming more fierce. This increased competition will largely benefit the semiconductor industry's evolution speed, as well as provide customers with cheaper and higher efficiency devices. Our project will not only encourage further development from competing companies and research groups, but also benefit BWRC's exploration of the utilization of DDR4's capabilities.

IP Strategy

The PHY interface provides us a good scope for creating a patentable Intellectual Property. The physical layer has been split into 5 major parts, each of which allow for novel implementations and innovations in circuit design. As we are working at the cutting edge of technology, we would have to adopt non-trivial techniques to meet the specifications for high data rates of DDR4. One or more of these implementations can provide us patentable IP. This section will discuss why this technology may be patentable, the advantages and disadvantages of seeking a patent, the current state of the semiconductor IP space, and the risks associated with not seeking a patent.

In the context of IP, creative designs and creative solutions fall cleanly under the category of patentable assets. In essence, the purpose for securing IP is to declare discernible ownership over a design or utility (USPTO, 2013). As an independent entity, we can draw benefits from securing patents and owning patents. The benefits we pose to secure range from monetary compensation to strategic industrial presence.

From a monetary perspective, owning patents allows our team to claim ownership to a recognizable asset. After incorporating our team as a legal entity, a patent opens us to the opportunity of being acquired. The proceeds from an acquisition could be used to finance additional ventures, which our team currently does not have the financial freedom to pursue.

A secondary monetization strategy that patent ownership affords us, is the option to license our technology to independent entities who wish to avoid committing R&D expenses for the purpose of developing said technology independently. Aside from the legal expense that we would need to undertake, the licensing option is financially robust.

The third and final benefit is an unquantifiable benefit. The third benefit arises from establishing a reputation as an entity. Acquiring a patent will demonstrate that we, as a team, know how to drive concepts into patentable ideas, and patentable ideas into awarded patents. Successfully acquiring a patent will demonstrate to that we are capable as a team, and will instill external confidence into our capabilities. This reputation will position us to open new leads amongst skeptical and risk averse customers.

The disadvantage of applying patent is obvious: it burns money. Filing a patent is not as simple as people imagine. Normally attorney fee becomes a big piece of the cost. Determined by the type of invention, the attorney fees are range from $5000 to more than

$15,000(Quinn, 2011). Adding the government filing fee and all kinds of application fees, the total cost of preparing and filing a patent may exceed ten or twenty thousand dollars. In addition, the maintenance fees would be another big part of the cost. Depends on how many years the owner wants to keep, the maintenance fees float from $490 for small entities and $980 for large entities due at 3.5 years to $2055 for small entities and $4110 for large entities due at 11.5 years (Stim, 2012).

Considering that this IP would be used only for research or instructional purpose, it would be non-profitable. Therefore, applying for a patent brings financial burden to the owner. In other words, it would not be worth for individuals to applying patent for this IP. However, if the owner switches from individuals to college or Berkeley Wireless Research Center (BWRC), the conclusion would be different. First of all, the college or lab has budget to cover the cost. Furthermore, the patent would bring them reputation, which is far more important than profit for them. Thus, it would be worth to apply a patent for this IP for BWRC (note that BWRC happens to exists entirely in the public domain so it does not apply for patents, but a patent may be appropriate for similar institutions).

Unfortunately, the semiconductor IP market can be difficult for smaller entrants like us. The rate of patent enforcement by larger corporations has not increased over the past few decades (Hall 2007, 5). However, in attempts to increase market share and presence, they have increased the number of patents they file. In the 1980's, the median number of patents filed by an employee was less than one, whereas during the turn of the century it was near eight (Hall 2007, 10). While larger corporations have a broad and ever expanding portfolio, smaller firms focus on particular market segments in attempts to perfect and own this portion of the total revenue stream. Unfortunately for these smaller

firms, this means that if and when larger corporations expand into their territory, they have no choice to defend what little they have. It is for this reason that smaller firms tend to more be more aggressive in enforcing their patents (Hall 2007, 3). Thus, it can be expected that we would have to actively enforce our patent. If our patent (or patents) focused solely on DDR4 memory control and interfacing, then we would have no choice but to defend the few eggs in our basket.

The risks associated with not patenting the design are significant. Since the integrated circuit design is based on following certain physical requirement and universal specifications, hundreds of similar design and product can be invented in the short time of period based on a same standard. In DDR4 memory design particularly, JEDEC standard is the critical specifications that everyone need to comply. There is high possibility that other individuals or companies will come up with very similar or even the same design. As Gene indicated in his article, engineers who are working on solving a certain problem "are likely to find solutions that are similar" (Gene 2009:8). If a similar design is first patented by other entities, the potential financial loss is irreparable and a great amount design effort would be wasted. Furthermore, without patent the design appropriately, competitors and free-riders can easily take advantage of the design or embedded our inventions into their products without any recognition of our work and having any consequence. Besides these two factors, without right patenting, it is almost impossible to conduct technology transferring or licensing. And this would greatly impede the process of commercialization of the invention or designs.

Therefore, there are a great number of critical risks involving in not patenting the design and our memory controller design should be patented when its major functions and

specification are met. The management of the patent can be done via creating a patent portfolio. By using management software or having regularly review, updates, categorization and balancing of the patent portfolio, the management with quality could be achieved.

Trade secret is one kind of intellectual property with unlimited time of protection. It can be one method to protect our technology, but it is not the optimal. The DDR technology evolves every three years averagely, an unlimited protection time is unnecessary. Giving the fact that circuit design industry is highly standardized and reverse engineering of circuit is quite mature, it would be difficult to protect the design with only trade secret but not patent since the trade secret sufferers from commercial espionage and high cost of protection. Moreover, the trade secret cannot prevent the similar or same product from being designed. Due the nature of the circuit design industry, trade secret won't play an excellent role in limiting other similar designs. As Shane said, patent is able to "protects your rights regardless of what anyone subsequently develops" (Shane 2007:8). Therefore, for technological inventions such as circuit design, patenting would be the optimal method to protect its originality.

Ultimately, deciding whether to seek or not to seek a patent for our design depends on the novelty of the the final product. If we discover and implement a new physical layer architecture that provides performance, costs, and/or feature improvements over the competition, then the patent's value overcomes the cost associated with filing it. If the final outcome is unique, but provides only marginal benefits compared to the competition, then there will be no benefit in filing the patent.

Technical Contribution

The physical interface is divided into five sub-systems. They are serializer, transmitter, receiver, deserializer and timing blocks respectively as the block diagram present in figure 1. Each team member is responsible for designing and testing one of the functional blocks. Kyle, Miron and Kalika are working on the design of the serializer, deserializer and receiver respectively. I am majorly designing the transmitter and Sinan is in charge of implementing the timing block. The division of the block is based on the technical background and familiarity of the topic for each team member. All five blocks are critical for the interface to perform the required functionality.
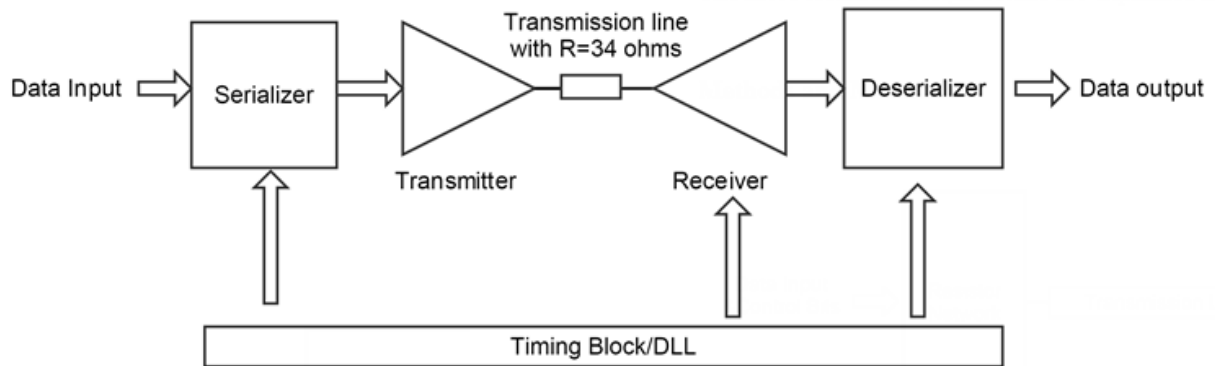
Figure 1. Memory interface design block diagram

Since the digital signal needs to travel through PCB trace or long wires, without signal integrity improvement and amplification, the signal would be significantly distorted and causing incorrect data interpretation on the receiver side. Therefore, the transmitter is an essential component not only for the interface but also for the quality of entire memory

controller communication. My individual work contributes to the completion of the interface design.

Literature Review

Since the DDR4 memory controller and its interface are sophisticated systems, in order to gain a good insight into its design mechanism, a great amount of the literature review was conducted for both topics. During the first phase, the state machine, commend instructions and configurations of the controller were researched via reading the DDR4 JEDEC STANDARD. After gaining the basic knowledge about the controller's functional mechanism, I started the literature review of the transmitter design inside memory interface.

The transmitter is also sometimes referred as the final stage driver because its nature of enhancing the signal and its position in the interface circuit. One of the most important concepts during design the transmitter is the On-Die Termination (ODT). As Michael indicated in his article, "any pulse or signal propagating along a bus will reflect from any part that is different" (Michael 2002:1). When the impedance along a transmission line is not unified, there will be some reflections occur on the impedance mismatch intersection. The reflection signal may encounter the original signal and "cancel each other out or cause some other interferences" (Michael 2002:1). The fundamental goal of the ODT is to "keep any reflections as small as possible" (Michael 2002:1). Providing the appropriate ODT is one of the prime goals of a transmitter so the signal interference can be mitigated.

Furthermore, as for the output swing, the paper written by Hsueh et al. indicated that the output swing of DDR4 driver is 660mV (Hsueh et al., 2014:fig.26.4.6) and the output

signal range is from 540 mV to top rail 1.2V according to the figures from the paper (Hsueh et al., 2014:fig.26.4.3). This fact was also indicated by the paper written by Nam, Daniel, Rohan and Nanju, who stated that in DDR4 driver, the out signal can "swing up to Vddq for 'high' and down to Vil for 'low' " where the Vil is determined by the termination resistance (Nam et al. 2010:1).

After understanding the design goals, I started to conduct the research on several design schematics. A DDR4 CA (Command and Address) buffers design was introduced in order to solve the problem that when the data rate increased, "the eye opening of the signal at the receiver end is not wide enough to meet voltage and timing requirement" (Kyomin et al., 2013:170). In this paper, a feedback dynamic control system was analyzed. The reference voltage feed into the buffer is "controlled more dynamically" (Kyomin et al., 2013: 170) by having a small portion of the input signal superposed on its original bias reference voltage.

A straightforward transmitter design was studied in the paper written by Nam, Daniel, Rohan and Nanju. This paper compared three different driver designs using pull-up and pull-down resistor network. The method of dynamically adjusting the resistor network connected based on transition stage of bits was first introduced. The paper also gave a detailed analysis on the resistor value selection associated with the transmitter's performance in terms of output swing and energy consumption. Moreover, the paper written by Hsueh et al. introduced a DDR4 differential and Dual-mode transmitter design. The impedance matching mechanism is similar to the one discussed by Nam, Daniel, Rohan and Nanju. Furthermore, the paper analyzed the advantage of using active devices

for impedance matching purpose. As the paper indicated, by using "parallel combination of complementary P/N, diode-/triode-region devices" (Hsueh et al., 2014:3), the transmitter can "achieve driver/on-die termination (ODT) linearity without the use of area-intensive passive resistors" (Hsueh et al., 2014:3).

The design of the driver circuit varies significantly depends on different system specifications and the design process consists of four stages. First stage is to select most effective and popular designs using by industry for DDR controller interface via literature review. Second phase is to understand the technical specification, implementation limits and characteristics of each selected method. Afterwards, modifications and improvements of existing designs are conducted in order to make the block better fitting into the system developed by our team and the last step is checking the compatibility with other direct connected blocks, that is, the serializer and the receiver.

Methods and Materials

Three main factors should be considered for a transmitter design. First factor is the impedance matching with transmission line. As the previous literature review explained, the impedance along a transmission line carrying a high frequency need to keep unified. Any mismatch on impedance would cause significant signal distortion and weakens signal strength at the receiver side. Thus, impedance matching becomes the prime goal for the transmitter. Second important factor is the signal virtual "common mode" voltage. For DDR4 driver, based on previous paragraphs' discussion, the output swing need to be set to 540mV to 1.2V, which is considered to be inside the "high side" voltage and giving a 870mV nominal "common mode" voltage. This relatively high nominal "common mode"

voltage would be beneficial to drive a NMOS device on the receiver side since the N type device need a high gate voltage to be activated. For current-mode transmitter, this voltage would determine the value of the current source and further define the power consumption of the transmitter.

The prime design idea was built based on the method proposed by the paper written by Nam, Daniel, Rohan and Nanju. There are a number of differences and modifications made in my design, which are the customized resistor combination selection implemented by a set of control signal and the output voltage swing from 540mV to 1.2V. The control signal sets are pre-programmed into another block based on the transmission line impedance change influenced by environment factors such as temperature and pressure.

Considered these factors, the single-ended transmitter design is shown in figure 2 below. The input includes input digital data and control signal. The output is the adjusted data signal along with a matched input impedance and designated output swing.
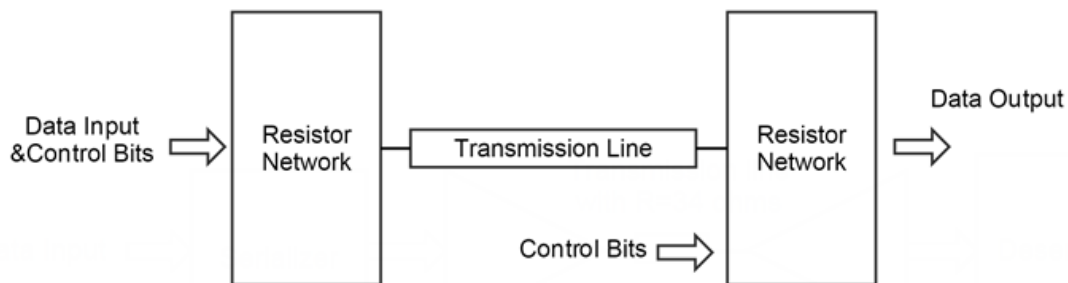
Figure 2. Systematic block diagram for the driver design
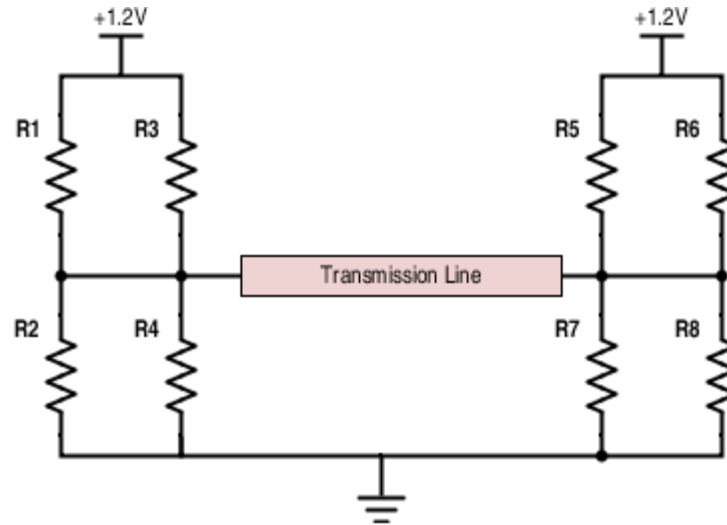
Figure 3. Resistor network example for the driver design

A circuit level design is shown in figure 3 below. Four pairs of resistor are included in this design. The first pair, R1 and R2 is mainly used to pull up the output voltage when the signal has a transition from low to high voltage. The second pair, R3 and R4 is connected into the network when the signal changed from high to low voltage. The third pair, R5 and R7 is the termination when the output signal is pulled up to high. The fourth pair R6 and R8 is the termination when the output signal is pulled down to low.

As figure 4 shows, the pair R1 R2, R5 R7 are connected to the network together when the signal goes high, that is, 1.2 V. In order to obtain a high rail voltage on the output terminal, ideally, R1 and R5 should directly connected to the 1.2V rail with the matching impedance value while R2 and R7 are left open. However, a ground path has to be provided via R2 and R7 due to the simulation convergence requirement of the circuit model. Therefore, R2, R7 need to have much larger values compared to R1 and R5 respectively in order to achieve a 1.2V output. Furthermore, the Thevenin equivalent of R1, R2 and R5,

R7 have to be equal to the transmission line characteristic impedance in order to reduce the reflection on the transmission line. According to data recommended by JEDEC, DDR4 driver supports two pull-up/down resistance values, either 34 Ω or 48 Ω based on either weak and strong modes (JEDEC 2012: 160-161). The pull-up/down resistance values are corresponding to the transmission line impedance, which indicates typical transmission line impedance is also either 34Ω or 48Ω. In this paper, the value of 34Ω will be used for all the analysis. In addition, in the paper written by Nam, Daniel, Rohan and Nanju, the value 40Ω was used to represent the transmission line impedance, which proves the validity of the 34Ω assumption.
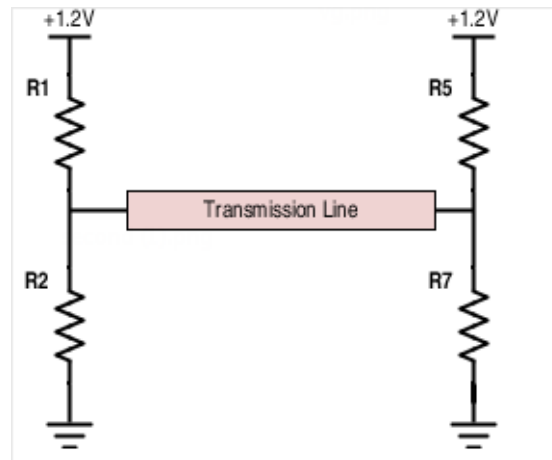
Figure 5. Resistor network example for pulling up circuit

When the output need to be pull down to 540mV. R3 R4, R6 R8 are connected into the network while the R1 R2, R5 R7 are disconnected from the network. Similarly, the value of R3, R4 and R6, R8 need to be calculated so that their equivalent impedance is equal to the transmission line impedance while achieving the 540mV voltage dividing on the output terminal as figure 6 shows.
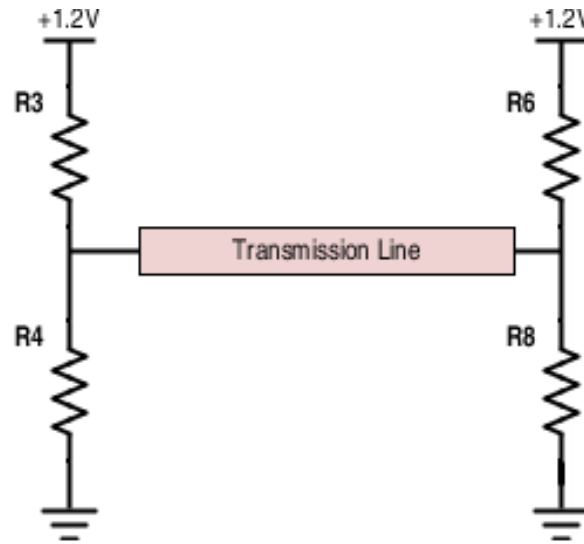
Figure 6. Resistor network example for pulling down circuit

Knowing the transmission line impedance of a typical DDR4 mother board is 34 Ω, we can use an ideal transmission line model shown in figure 7 and figure 8 for the analysis.
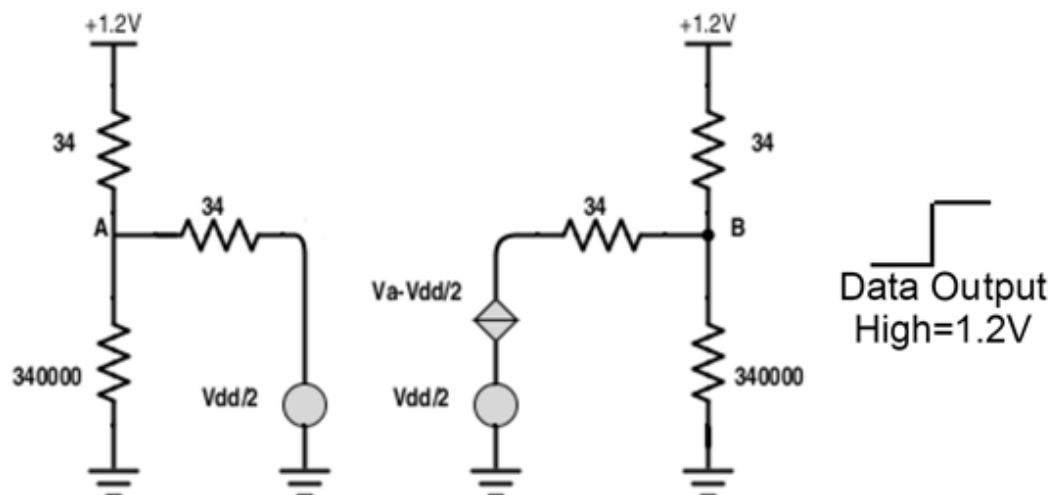

Figure 7. Pull-up network with ideal transmission line model

The model contains two characteristic impedance, two independent source with the voltage of $\frac{Vdd}{2}$ and one voltage controlled voltage source which has a value of $Va - \frac{Vdd}{2}$. Va is defined as the voltage at the node "A" shown in figure 7 and 8.

In order to configure the output voltage level as well as match the transmission line impedance, according to the discussion from previous paragraphs, we set the value of R2, R7 10000 times larger than R1, R5 respectively and keep their Thevenin equivalent to 34 Ω.

$$R_2 = 10000R_1 \qquad R_7 = 10000R_5$$
$$34 = \frac{R_2 \times R_1}{R_2 + R_1} \qquad 34 = \frac{R_7 \times R_5}{R_7 + R_5}$$

From solving the equation above, we obtain the value for the pull up circuit resistance which is $R_2 = R_7 \approx 340000\Omega, R_1 = R_5 \approx 34\Omega$.
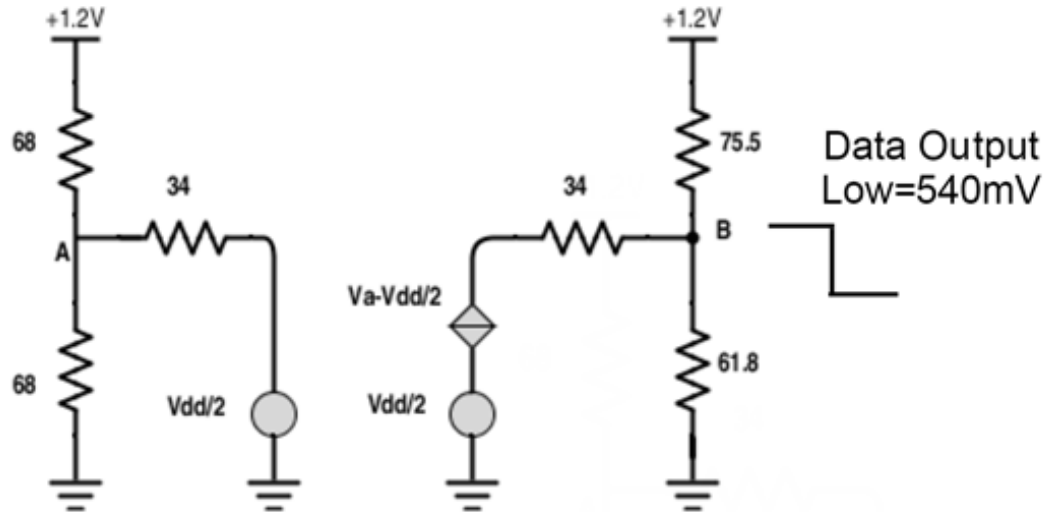
Figure 8. Pull-down network with ideal transmission line model

Similarly, by using the same transmission line model, we can also obtain the resistance of R3, R4 and R6, R8 in order to achieve 540mV output voltage while keeping the equivalent impedance matched with 34Ω line impedance.

$$540mV = \frac{1.2 \times R_8}{R_6 + R_8}$$

$$34 = \frac{R_6 \times R_8}{R_6 + R_8}$$

The value we obtained are $R_6 \approx 75.5\Omega, R_8 \approx 61.8\Omega$. Moreover, R_3, R_4 are designed to be 68Ω respectively so that their Thevenin equivalents are 34 Ω on both sides of the transmission line and Va is 0.6V as shown in figure 8.
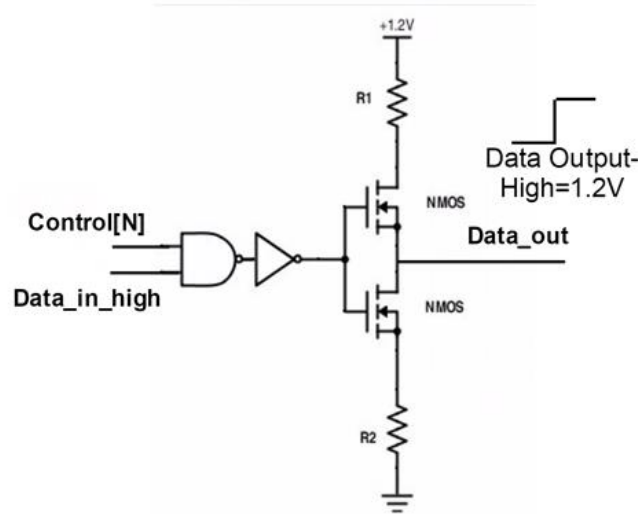
Figure 9. Circuit implementation of pulling up resistor pair

Inside the Verilog-A model, the implementation of enabling/disabling the resistor is achieved by using the nested "if" statement. In the physical circuit, the functionality could be completed by using NAND , NOT gates and MOSFET. The NMOS circuit shown in

figure 9 would enter the triode region only when both "Data_in" and "Control bit" become high. The PMOS circuit shown in figure 10 would enter the triode region only when "Data_in" goes low and "Control bit" becomes high.
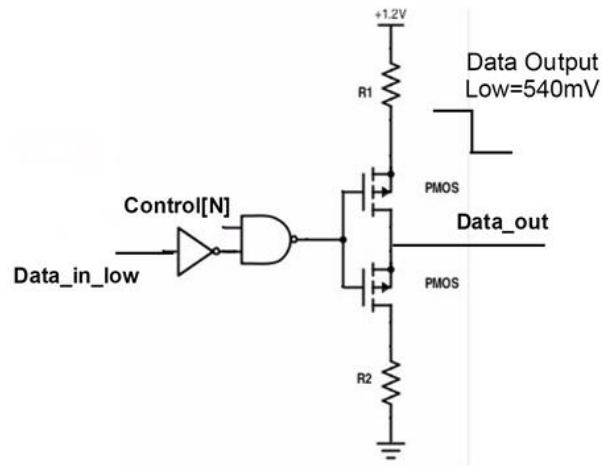
Figure 10. Circuit implementation of pulling down resistor pair

The control signal is essentially a disable/enable signal. When its value is high, the designed resistor pairs will be connected into the network. When it becomes low, the corresponding MOSFETs turn off and the resistor pair will be cut offline.
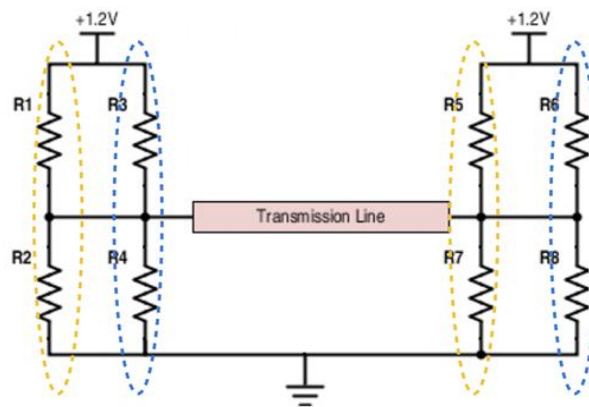
Figure 11. Control illustration of the resistor connection

As figure 11 indicates, the pulling up resistor pairs circled in orange would be controlled by one designated control bit and the pulling down resistor pairs circled in blue will be controlled by another designated bit. In order to complete the required output voltage swing and impedance matching, one pulling up pairs and one pulling down pairs are required to remain activated while the entire operation. Since transmission line impedance varies with environment factors, having the control bits enables the driver to adjust its output impedance to achieve best match result. By connecting more pairs pulling up/down resistor pairs into the network, the adjustment of the output driver impedance can be implemented.

There is an alternative version of the transmitter line model implemented during the design process, which is to model the transmission line as a resistor under the DC input condition.
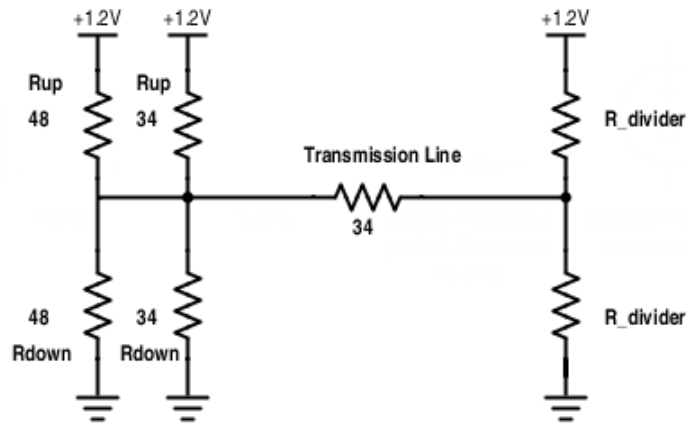

Figure 12. Driver design with modeling the transmission line as resistance

Similarly to the previous model, the termination equivalent resistance need to be the same as the line impedance.
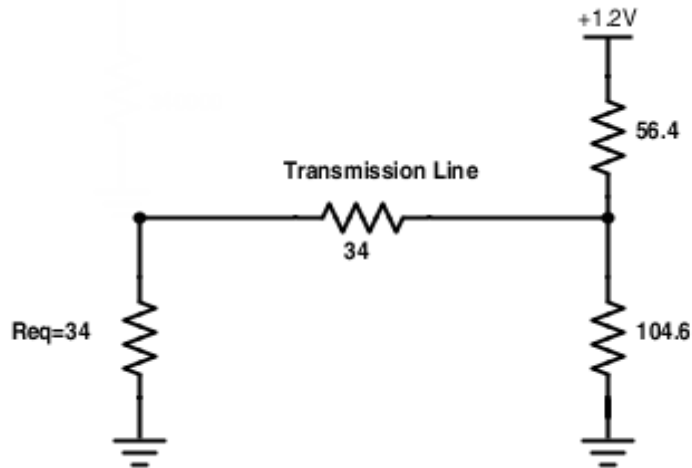
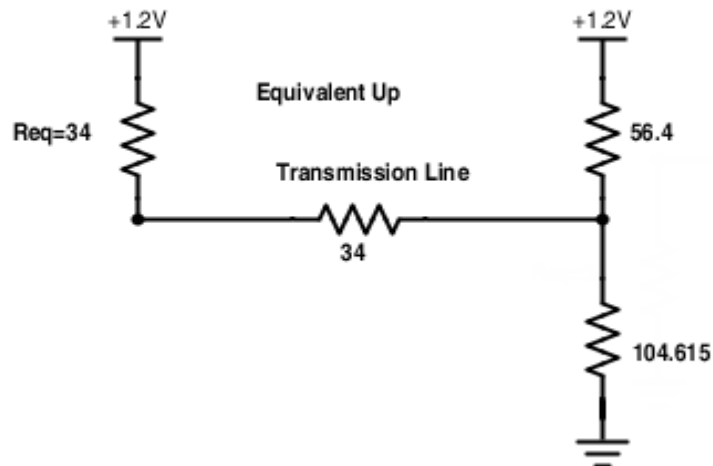Figure 13.Pull down circuit with modeling the transmission line as resistance

Figure 14. Pull up circuit with modeling the transmission line as resistance

Based on the schematic shown in figure 13 and figure 14, the resistor used in the voltage divider can be calculated using KCL at the output node. The line impedance is assumed to be 34Ω. In order to achieve the output swing from 540mV to 1.2V while

keeping the output impedance matched with line impedance, as the number shown in figure 13 and 14, resistors used in the termination voltage divider is calculated as $R_{high} \approx 56.4\Omega$, $R_{down} \approx 104.6\Omega$. The simulation result for both models are discussed in the following section.

Results and Discussion

The final output stage driver is mainly a circuit model aiming to provide an adjustable impedance matching network and to provide designed output voltage swing. The following pictures show the simulation result of the circuit with modeling the transmission line as dependent and independent voltage sources. From figure 15, we can observe that the output waveform (green) follows the input (ideal voltage pulse in red) perfectly and the low voltage is adjusted to 549.998mV and the high voltage is 1.199V.
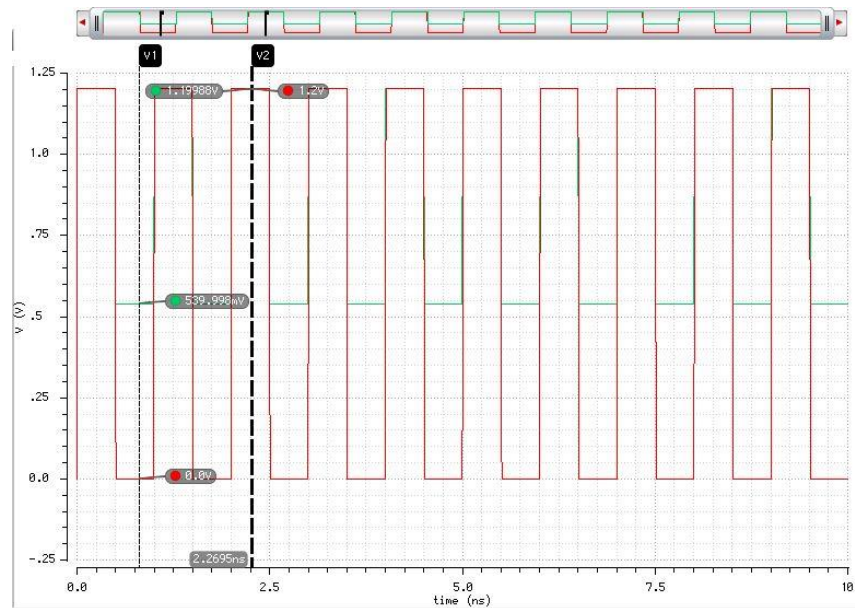

Figure 15. Test bench Input &Output waveform with independent & dependent voltage

source transmission line model

Figure 16 and figure 17. shows the joint simulation result with the serializer. The red curver is the input from the serializer and the green curve represents the output waveform from the driver. The sample points are taken with 20ps apart from the center which is defined by the point when input is acoorsing 600mV. From the figure we can observe the output waveform becomes shaper and the low voltage is adjusted to 549.9mV while the input is 4.9mV. The output high voltage is 1.19V while the actual intput from serializer is 1.19V as well.
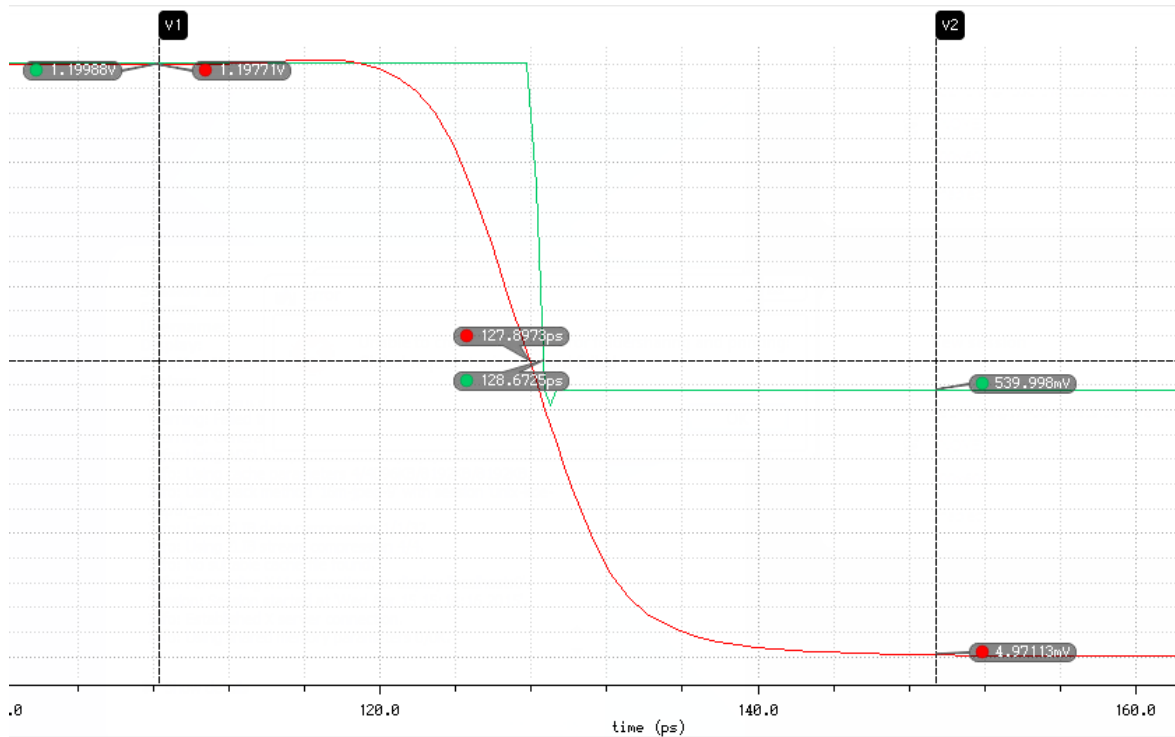

Figure 16. Integrated test bench result of the circuit with independent & dependent

voltage source transmission line model

The similar result can be obtained when the input falling. The sample points are taken with 20ps apart from the center which is defined by the point when input is acoorsing

600mV. While the high input voltage is 1.18V, the output voltage from driver is 1.19V. Moreover, while the low input voltage is -2.02 mV, the low output voltage is adjusted to 549.98mV.
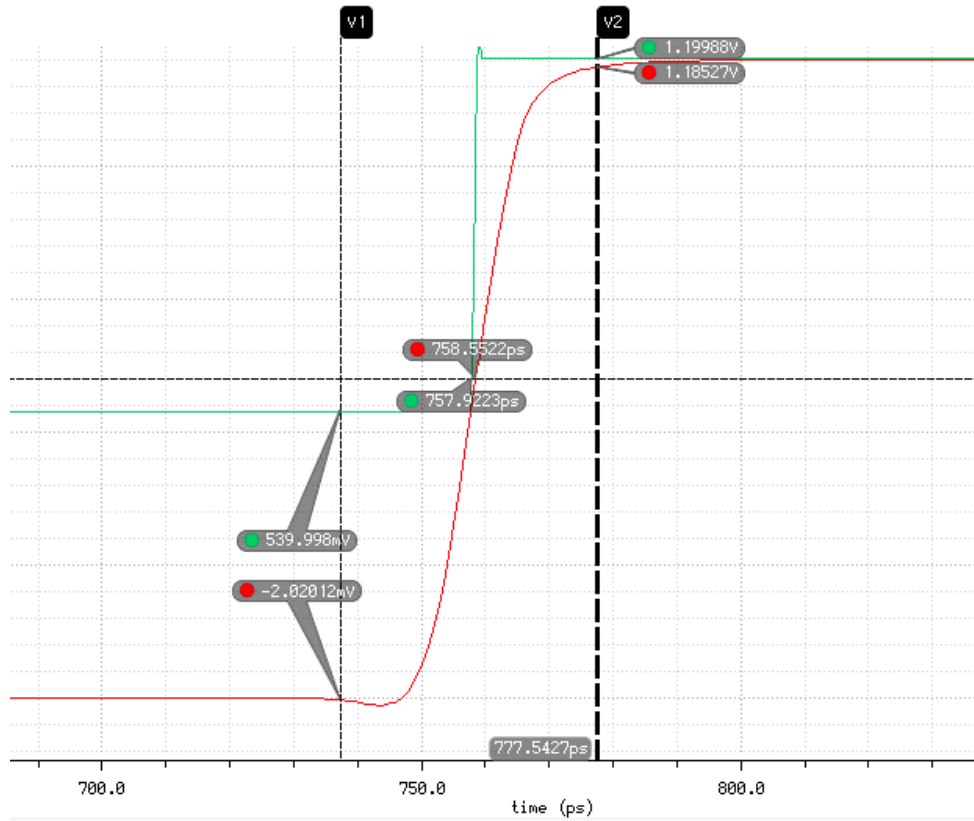

Figure 17. Integrated test bench result of the circuit with dependent voltage source transmission line model

The alternative circuit model with the resistor model of the transmission line is also tested. The following pictures show the simulation result tested under the ideal test bench and integrated system test bench.
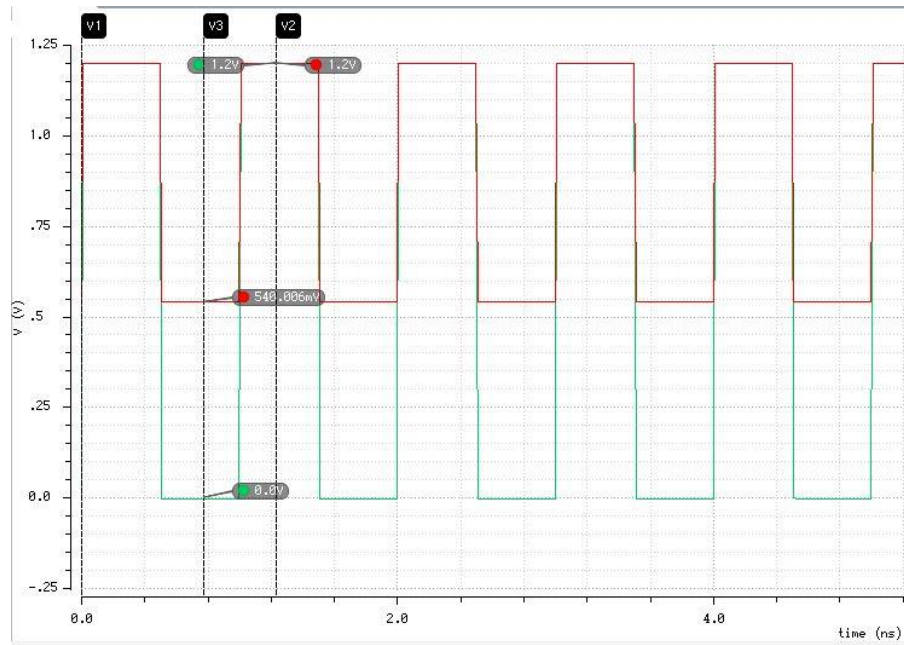
Figure 18. Test bench result of the circuit with resistor transmission line model
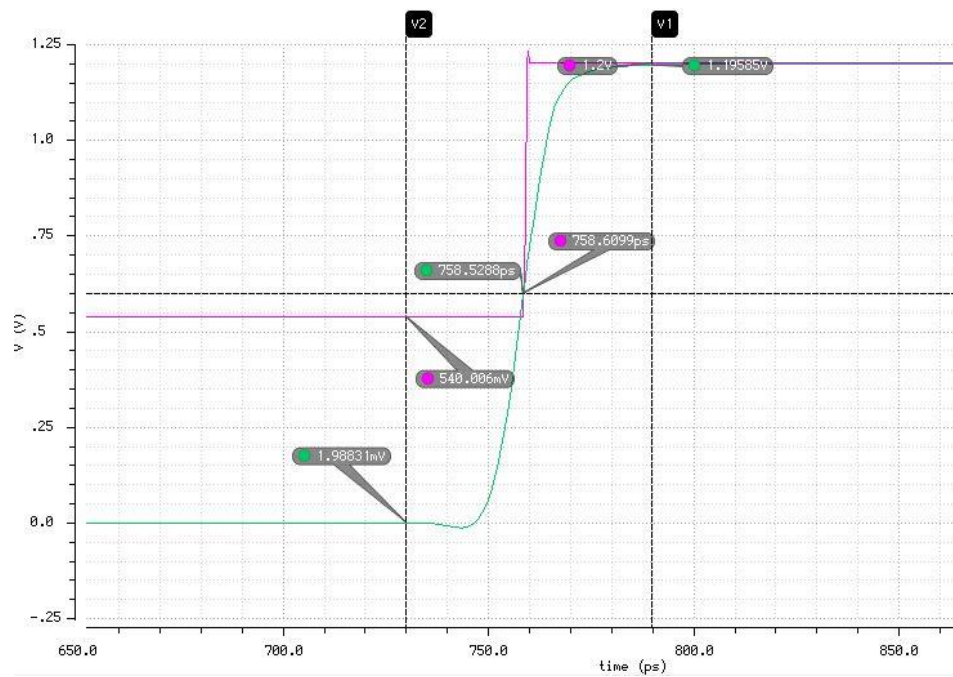

Figure 19. Integrated test bench result of the circuit with resistor transmission line model
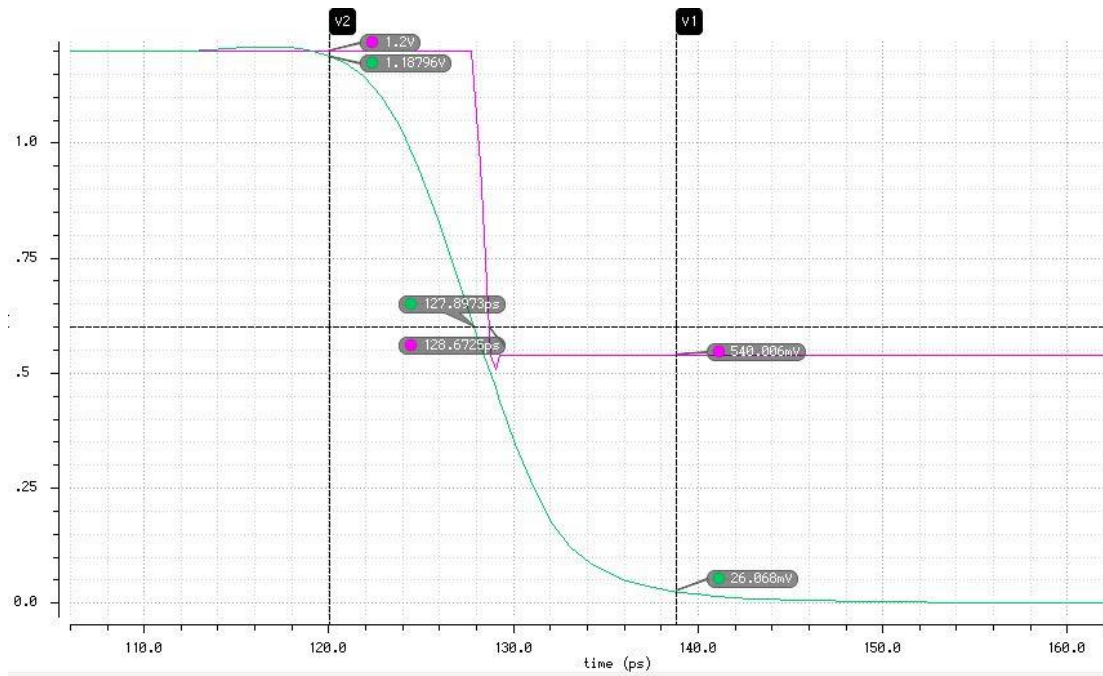
Figure 20. Integrated test bench result of the circuit with resistor transmission line model

The simulation result also indicate the validity of this model in terms of setting the output swing. As the figure 19 and 20 show, the red curve represent the output from the driver while the green curve is the driver's input acquired from the serializer. The sample points are taken with 20ps apart from the center which is defined by the point when input is acoorsing 600mV. When the input takes a transition from low to high, the high input voltage is 1.19V while the output voltage from driver is 1.20V. When the intput voltage goes to low with the voltage of 26.06mV, the the low output voltage from dirver is adjusted to 540.00mV. However, due to the limited ability of using resistor to model the transmission line, this model may not refelct the full behavior of the pulling up/down circuit as the previous circuit does. D

From the observation, although there are some some overshoot during the transition, the voltage level for both high and low voltage are evetaully setteled. By having the joint test bench, the compability and realibiltiy of the dirver block can be verified. The simulation result indicated that the final stage driver has implemented its design goal and specifications.

Concluding Reflections

In a nutshell, after the integrated system was tested, the goals of the designing the physical interface has been achieved. The simulation results emphasize the importance of having a designated transmitter block for the memory physical interface. The current outcomes has matched the designed functionality and performance expectation. From the participation of the entire capstone research, I learned several important lessons. The most important one is I have learned the necessity of quickly scoping the project down and located a tangible design target. A vague defined plan or design need to be quickly condensed and finalized to form an applicable design. Furthermore, I also gained a stronger ability of conducting self-research and implementations via using different tools since my familiarity of digital circuit was not abundant at the beginning. Via building the Verilog-A blocks in Cadence, I also learned how to use Cadence development tools, building test bench and simulating analog circuit in Verilog-A as well. With the great assistance from my teammate, the pace of the learning has been significantly boosted.

In terms of the future research, there are different stages of the implementation could be made. The current functionality of the final stage driver is implemented with Verilog-A. Although the pulling up/down circuit has been modeled, there are a few functions left

such as control enabling need to be implemented using circuit models. With different resistor combinations enabled by the control function, when the change of transmission line impedance is detected, a different set of output impedance could be applied to achieve better matching result. The feedback dynamic control of the output impedance could be another future challenge. In addition, on further stage, the entire system need to be translated into layout and taped out. If someone were to pick up from here, the recommended learning sequences would start from learning the key concept of the high speed communication link then studying about drawing the layout of the chip. Also, a deep understanding on DDR4 controlling mechanism would be also very beneficial.

The project put a large emphasis on self-design and learning process. From a vastly defined topic to a specific component, a great amount of research and discussion need to be done to better understand the object and handle the challenges. From this research, I have learned the process and approaches of the system level design as well as digital circuit design. Most importantly, I enhanced my knowledge in digital circuit domain by not only researching the material but also communicating with my teammates.

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