

Low Voltage Analog to Digital Converter Design in 90nm CMOS

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**Design of Low-Voltage Analog To Digital Converter in
submicron CMOS**

by Simone Gambini

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences,
University of California at Berkeley, in partial satisfaction of the requirements for
the degree of **Master of Science, Plan II.**

Approval for the Report and Comprehensive Examination:

Committee:

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* * * * *

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Date

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Chapter 1

Introduction

With Moore's law driving the cost of a square millimeter of silicon steadily down, the economic potential for electronics to become ubiquitous has appeared. In the last ten years, portable devices such as cell-phones, PDAs or laptops have first made their appearance in the market, to then continuously support increased functionality and *intelligence*. While the current spread of such devices is of the order of one or two per person⁽¹⁾, it is natural to think that the ongoing decrease of cost will enable electronic devices to be present in the environment with densities of tens, or maybe hundreds, per person. Such devices would not necessarily be allocated substantial computation power individually; however, when allowed to communicate, they could perform useful tasks such as online environment monitoring and response, distributed computation and similia. To minimize deployment cost and effort and minimize network adaptability and lifetime, the interconnection amongst nodes should happen over the air, without requiring any wiring. The electronic system described above is a Wireless Sensor Network (WSN) ([1], [2]). The major obstacle to the massive deployment of Wireless Sensor Networks has to do with power. Power dissipation dictates battery size, which has usually a substantial impact on electronic system size. Achieving a small enough size will be (and already is) in turn one of the discriminating factors in deciding whether such

¹At least in so-called developed countries

dense networks of electronic components will be a reality.

The ultimate choice in reduction of battery size is the removal of the battery, and the usage of circumstant environment as an energy source. This paradigm is usually referred to as energy scavenging([3]). Miniature vibration-to-electrical, or heat to electrical power converters subject of ongoing research are expected to be able to provide an average power in the order of tens of microwatts,introducing an extremely tight power constraints on any system using them as a primary power source.

Part of the power reduction necessary to meet the scavenging requirement can come from *functionality redistribution*:in a large enough network system-level optimizations can be exploited to ensure functionality,even in the case where individual nodes do not have large computational capabilities. The power savings obtainable through such system level decisions are however not sufficient to break the scavenging barrier, and must be reinforced with circuit-level innovations.

A sector where improvements in the state of art were necessary is the radio link. The observation that communication power, would most likely dominate the total node budget motivated several research efforts, including that of Otis,Chee,Pletcher and Prof.Rabaey at Berkeley, that of Cook,Molnar and Prof. Pister still at Berkeley and most recently, that of Gyselick and Ryckaert at IMEC. These efforts aimed at reducing the communication power to an extent where it would not be a concern for the total budget.

For different reasons, however,not all of these works addresses the design of the A/D converter. In [4], a UWB system is considered, where signal bandwidth and data-rate are large and power can be reduced through duty-cycling. An A/D converter with moderate power consumption and fast turn-on time provides therefore a viable solution. In [5] and in [6], FSK modulation is used, so that an ADC is not required neither for demodulation nor for synchronization.

For the system proposed in [7] instead, conversion of baseband signals into the digital domain enables the implementation of channel estimation and timing acquisition routines in digital. As described in [8], this results in shorter packet headers and lower system energy.

The design of an A/D converter suitable for sensor network radios is the topic of

this work. As we show in a following section, the specifications of a converter designed to be used in a radio system are different than those typically described in previous low-power data converter literature, which mostly target kilohertz-range, high resolution sensing applications.

In addition to meet the specifications dictated by cooperation with the radio, the converter should operate from an operating supply as low as possible, to facilitate integration with low-voltage, power efficient digital circuits. Therefore, results of this thesis also highlight some of the challenge that designers will face as technology nodes keep progressing.

1.1 Background on radios for wireless sensor networks developed in the picoradio project

The converter systems designed in this work were conceived as being complementary to the radios described in [9] and in [10]. Table 1.1 reports the key performance figures of these RF front-ends. These receivers operate according to different principles, even though their design was driven by the common goal of eliminating the power hungry local oscillator and using envelope-detection down-conversion. When this approach is taken, the major difficulty is to provide enough RF gain to suppress the high noise figure of the envelope detector. In a tuned-RF architecture ([9]), the gain is provided by conventional tuned-amplifiers; since providing RF gain is expensive, however, a sharp power-sensitivity tradeoff is present.

Super-regeneration([10]) on the other hand, allows to get very high RF gain by periodically modulating the loop-gain of a tuned oscillator. The baseband output of a receiver employing this architecture is a pulse-width-modulated signal, where the pulse duration depends logarithmically on the input signal. This pulse width modulated signal contains strong tones at the harmonics of the quench frequency. In [10], these tones are filtered by a third order Butterworth response to relax A/D conversion specification.

	[9]	[10]
Architecture	Tuned RF	SuperRegenerative
Sensitivity	-78dBm	-100dBm
Maximum Data Rate	100 Kbps	20Kbps
Modulation type	OOK	OOK
Power Dissipation	3mW	400 μ W

Table 1.1: Performance Summary for On-Off Keyed(OOK) wireless sensor networks radios

1.1.1 Converter performance requirements

In this section, we derive specifications for analog-to-digital converters to be used in wireless sensor receivers. These specifications are obtained through a MATLAB-based system-level analysis. First, radio [9] is considered.

The graph in figure 1.1 reports bit-error-rate versus ADC resolution for the radio receiver in [9]. This graph was obtained by simulating in MATLAB a simple model of the front-end, including digitization and matched filtering². For 50Kbs communication, an 8-bits, 750KS/s converter seems to provide satisfactory performance (BER=3e-3 @ -72dBm RF input, the simulated sensitivity limit). Similar performance can be achieved by preceding a 6-bits ADC with a 25dB gain stage. This gain stage should be made programmable to accommodate large inputs or interferers. This choice is regarded in [8] as suboptimal, as the training of a PGA would increase packet length and hence system energy consumption. Another set of constraints on ADC performance comes from the digital synchronization algorithm [8]. The algorithm assumes each packet bears a known header of 7 bits, and is based on a cross-correlation scheme. The digitized output of the receiver is oversampled by a factor of K and correlated against the upsampled version of the header sequence. From the properties of auto-correlation functions, the exact sampling interval can be estimated by the argmax of this cross-correlation.

²(Note that these figures are somewhat pessimistic because slicing was performed without prior timing acquisition, so the matched-filter output is sampled with an unknown delay w.r.t. the optimal instant)

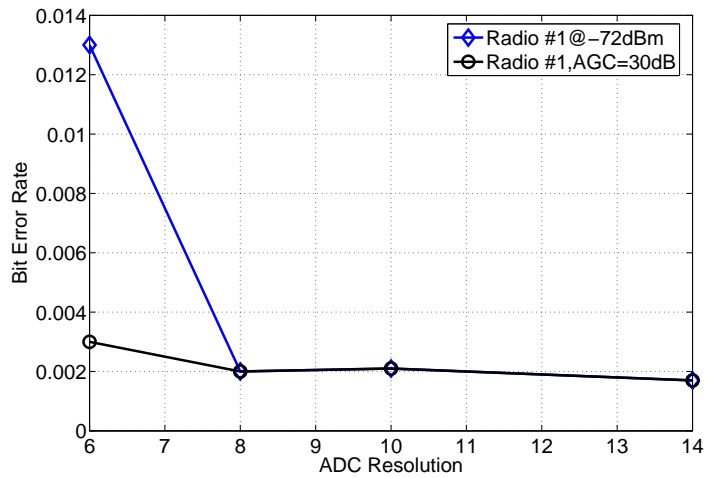


Figure 1.1: Simulated Bit Error of receiver in [9] versus ADC number of bits for data reception

The ADC introduces two non-idealities on this process: first, the finite amplitude resolution perturbs the calculation of the correlation peak; second, the finite timing resolution (K choices per bit interval are available instead of the whole continuum) results in quantization of the optimal estimated instant. According to [8] an ADC with 8 bits of resolution and 500KS/s sampling rate is sufficient with large margin. MATLAB simulations of the whole receiver chain, however, indicated the the amplitude resolution can be reduced to 6 bits without loss of performance(see figures 1.2-1.3) while sampling rate cannot be reduced below 500KS/s(OSR=5). A similar analysis can also be performed for the super-regenerative radio receiver of [10]³. Figure 1.4 shows the results the results of a series of behavioral simulations where bit-error rate is measured against versus ADC resolution at the simulated sensitivity level of -87dBm. The resulting minimum resolution for data reception is again 6 bits, with a reduced samplign rate requirement of $200KS/s$ (for 20Kbps data communication) . The requirements induced by the synchronization algorithm are similar to those of the previous radio. Table 1.2 reports the specifications derived for the companion converters of both receivers.

³A different front-end model is needed for this analysis

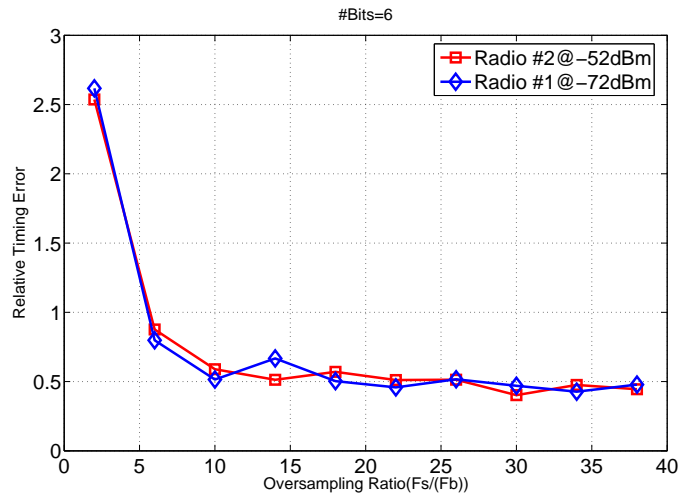


Figure 1.2: Timing estimate at the receiver as a function of the ADC oversampling ratio. The finite asymptote in the estimated delay is due to the phase-shift due to finite envelope-detector bandwidth

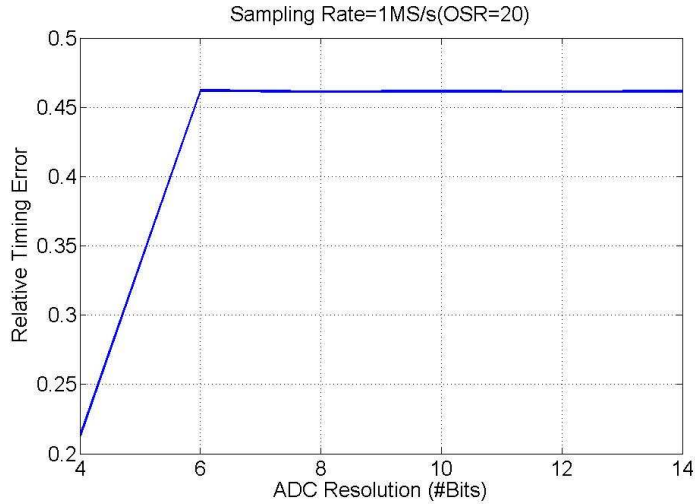


Figure 1.3: Timing estimate at the receiver as a function of the ADC resolution. The finite asymptote in the estimated delay is due to the phase-shift due to finite envelope-detector bandwidth

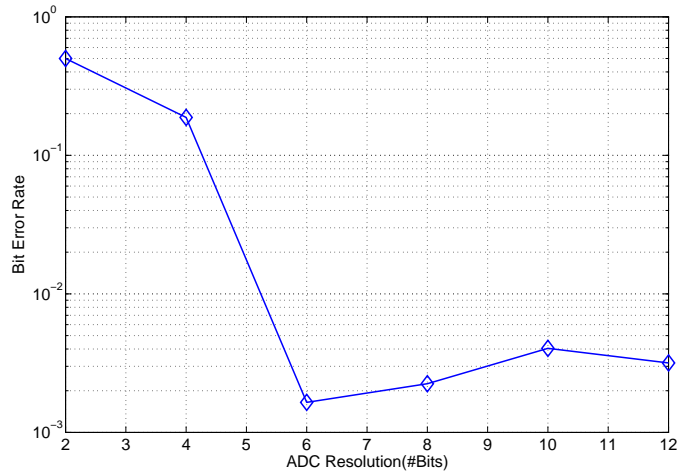


Figure 1.4: Simulated super-regenerative receiver Bit Error Rate versus ADC resolution

Radio	[9]	[10]
Resolution	8 bits(no AGC)/6 bits(25dB AGC)	6 bits
Sampling Rate	1MS/s	100KS/s
Power Dissipation (P_d)	$\leq 100\mu W$	$\leq 40\mu W$

Table 1.2: Summary of converter specifications

1.2 Thesis organization

In the next chapters, the realization of the specifications in table 1.2 is described. Chapter 2 covers the chosen design methodology, and introduces the main challenges for low-voltage, low-power designs in fineline technologies, namely reduced signal swing, reduced switch R_{off}/R_{on} ratio and degraded amplifier gain. The rest of this work describes the implementation of three different converters. In chapter 3, a first prototype successive approximation converter that resolves 6 bits at 1.5MS/s is described. Underestimated digital leakage dominates the power budget of this converter, which still consumes only $14\mu W$ from a 0.5V supply. In chapter 4, a revised 6 bits, 1MS/s successive approximation converter is described. This converter, which incorporates reference generation and distribution and is equipped with a mixed signal offset-cancellation routine, consumes $17\mu W$ of which only $6\mu W$ s are spent in the ADC core. Chapter 6 finally describes an experimental $\Sigma - \Delta$ modulator, designed to perform digital pulse width demodulation for the super-regenerative receiver [10]. This converter uses low-gain operational amplifier to minimize flicker and thermal noise and achieves over 65dB dynamic range in 50KHz bandwidth, while dissipating $27\mu W$. Conclusions are drawn in chapter 6.

Chapter 2

Design considerations for low-voltage analog/mixed-signal circuits

In this chapter, we develop a framework to perform low-power, low-voltage design. As a first step, we fit a current mode compact model to the active devices available in this process. After briefly discussing the fundamental limitations of analog design, i.e. thermal noise and device mismatch, we analyze the bottlenecks in the design of the principal mixed-signal building blocks such as switches, comparators and operational amplifiers at low operating supplies, identifying the major challenges and devising possible strategies to overcome them.

Finally, we move one step forward in the abstraction hierarchy to consider power efficient converter architectures.

2.1 Process Technology

The designs described in this thesis were realized using a 90nm feature size CMOS technology with a peak transition frequency $f_t^{(max)}$ of the order of 100GHz. At

the MHz operating frequencies used in this work, the ratio $f_t^{(max)}/F_s$ is a few tens of thousands; even if we restrict ourselves to the case $V_{dd} = 0.5V$, the peak f_t remains of the order of the tens of GHz and the aforementioned ratio a few thousands. Clearly, the process intrinsic speed capabilities are almost infinite compared to the applications needs. The increased baseline speed however, is accompanied by lower device intrinsic gain due to shorter channel length and by decreased stacking capability, and hence per amplifier-stage gain, due to reduced supply. Furthermore, gate and drain leakage and flicker noise are much increased. These characteristics naturally favor high-speed applications with small signal swings and small precision requirements (i.e. RF circuits). In a certain sense, as the process gets faster, the minimum frequency at which it can be efficiently used quickly increases. This trend is bound to continue/worsen over the next technological nodes, and is already inducing some fundamental change in the way analog circuits are designed [11].

2.1.1 MOSFET model

Throughout this work, we use a current-based MOSFET model known as ACM model [12]. This model bears a high degree of resemblance to the EKV [13] model, with which it shares the current-based approach. It is our belief that this category of models is better suited to represent the intrinsic active device characteristics in the weak and moderate inversion regions, that are typically used in low-power design. Also, a current-based model more closely reflects the practice of circuit design, in which devices are more often current biased than voltage biased.

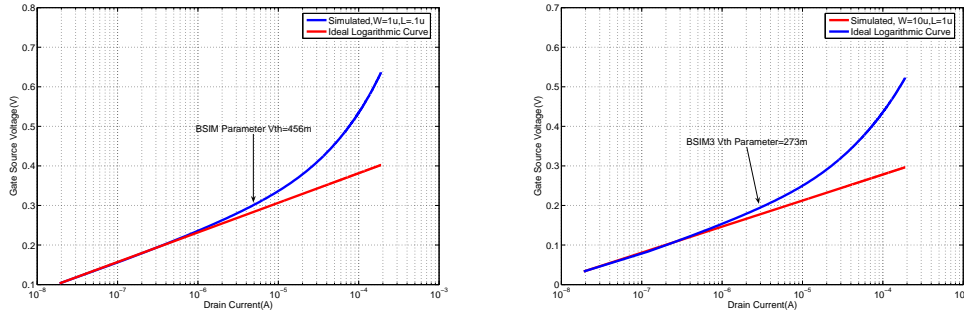


Figure 2.1: Simulated $V_{gs} - I_d$ curves of a diode connected device for a short and a long channel device. The reverse short channel effect affecting the longer device is apparent in this figure

2.1.2 Small signal gain and capacitance

The ACM expressions for C_{gs}^i and G_m of a are reported below.

$$G_m = \frac{2I_d}{nV_{th}} \frac{\sqrt{1+IC} - 1}{IC} \quad (2.1)$$

$$C_{gs} = \frac{2C_{ox}WL}{3} \cdot \frac{q(q+3)}{(q+2)^2} \quad (2.2)$$

$$q = \sqrt{1+IC} - 1 \quad (2.3)$$

$$IC = \frac{I_d}{I_s} \quad (2.4)$$

$$V_{th} = \frac{KT}{q} \quad (2.5)$$

The model is parametrized in terms of $I_0 = 2\mu_n C_{ox} (nV_{th})^2$, the current predicted from the quadratic model of the mosfet when $V_{gs} = V_t + 2nV_{th}$, i.e. at the edge of moderate inversion. There are several way to obtain a value for I_0 for a given technology. A naive one is to measure¹ the (semilogarithmic) $I_d - V_{gs}$ characteristic of a diode connected device. As long as the current is low enough to keep the device in weak inversion, such characteristic is a straight line; while it becomes an exponential in strong inversion. The result of two such simulations, respectively for a short and a long channel devices, are shown in figure 2.1. For this technology this method results in $I_0 \approx 1\mu A$ for NMOS, $I_0 \approx .3\mu A$ for PMOS. As seen in

¹in this paragraph, the word measurement is used to refer to any procedure regarded as reference, either simulation through a device simulator or BSIM models or actual measurement

figure 2.1, however, the transition from weak to strong inversion is smooth, so that the selection of a single point as separator is error-prone. Therefore, this method can only be used for a quick estimate of the model parameter I_0 .

A more accurate way to extract I_0 is described in [14]. When circuit in figure 2.2 is considered, it can be shown that the slope S of the $\sqrt{I_d} - V_s$ curve, extracted when the device is in strong-inversion, equals $\frac{\sqrt{I_0}}{n \cdot V_{th}}$. Therefore, S is measured through a DC sweep, and I_0 can be calculated as

$$I_0 = (S \cdot n \cdot V_{th})^2 \quad (2.6)$$

(n can be extracted separately through a simple $I_d - V_{gs}$ simulation in subthreshold). For the given process, extraction results are summarized in table 2.1. Finally,

Polarity	L	n	I_0
<i>N</i>	.1 μ	1.5	.167 μA
<i>N</i>	1 μ	1.35	.25 μA
<i>N(CFT)</i>	.1 μ	1.15	.13 μA
<i>N(CFT)</i>	1 μ	1.5	.37 μA
<i>P</i>	.1 μ	1.5	38nA
<i>P</i>	1 μ	1.5	34nA
<i>P(CFT)</i>	.1 μ	1.5	63nA
<i>P(CFT)</i>	1 μ	1.15	48nA

Table 2.1: MOSFET model as extracted from simulations

one can choose to determine model parameters through curve fitting, having the further degrees of freedom of what data to use for the fit, and what parameters to fit versus what to measure are added. In this work we estimated the model parameter through curve fitting using data from the transconductance versus bias current of a diode connected device. The circuit is shown in figure 2.2. The device has $W/L = 10$, while the bias current I_d is varied between 10nA and 200 μA . MATLAB lsqcurvefit routine was then used to determine the values for parameters I_0 and n . As shown in figure 2.3, both extraction after [14] and fitting result in excellent agreement with full BSIM simulation, showing that both the model equation and the extraction procedure described in [14] are sound and can be used

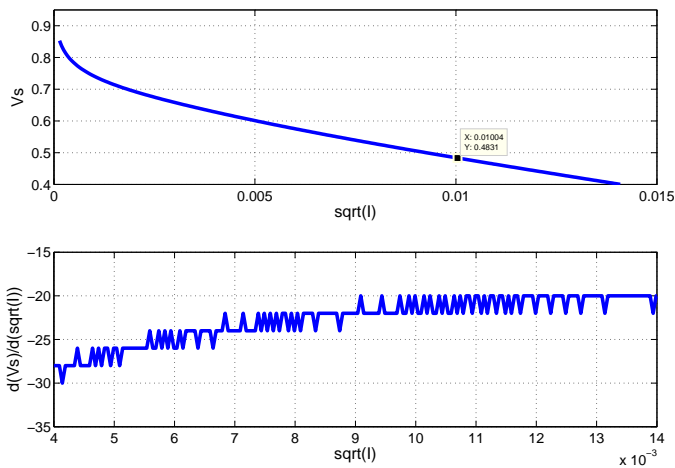
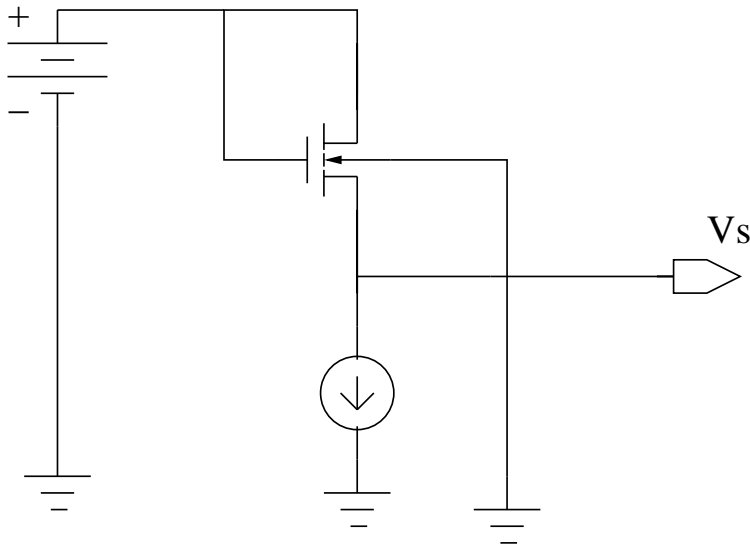


Figure 2.2: Circuit to extract the specific current of a device(top) and typical $\sqrt{I} - V_s$ curve(bottom).

even at the 90nm technological node.

Since I_0 is the only parameter in the model, the value determined previously should be used also to compute the bias-dependent gate-source capacitance C_{gs} . Oxide capacitance per unit area C_{ox} , overlap capacitance per unit width C_{ol} and effective length L_{eff} are the additional parameters needed for this calculation. Since such values are typically reported in the process manual, the value of C_{gs} can be directly calculated once I_0 is known. As reported in figure 2.5, this method guarantees a 30% worst case accuracy for C_{gs} . The accuracy can be improved

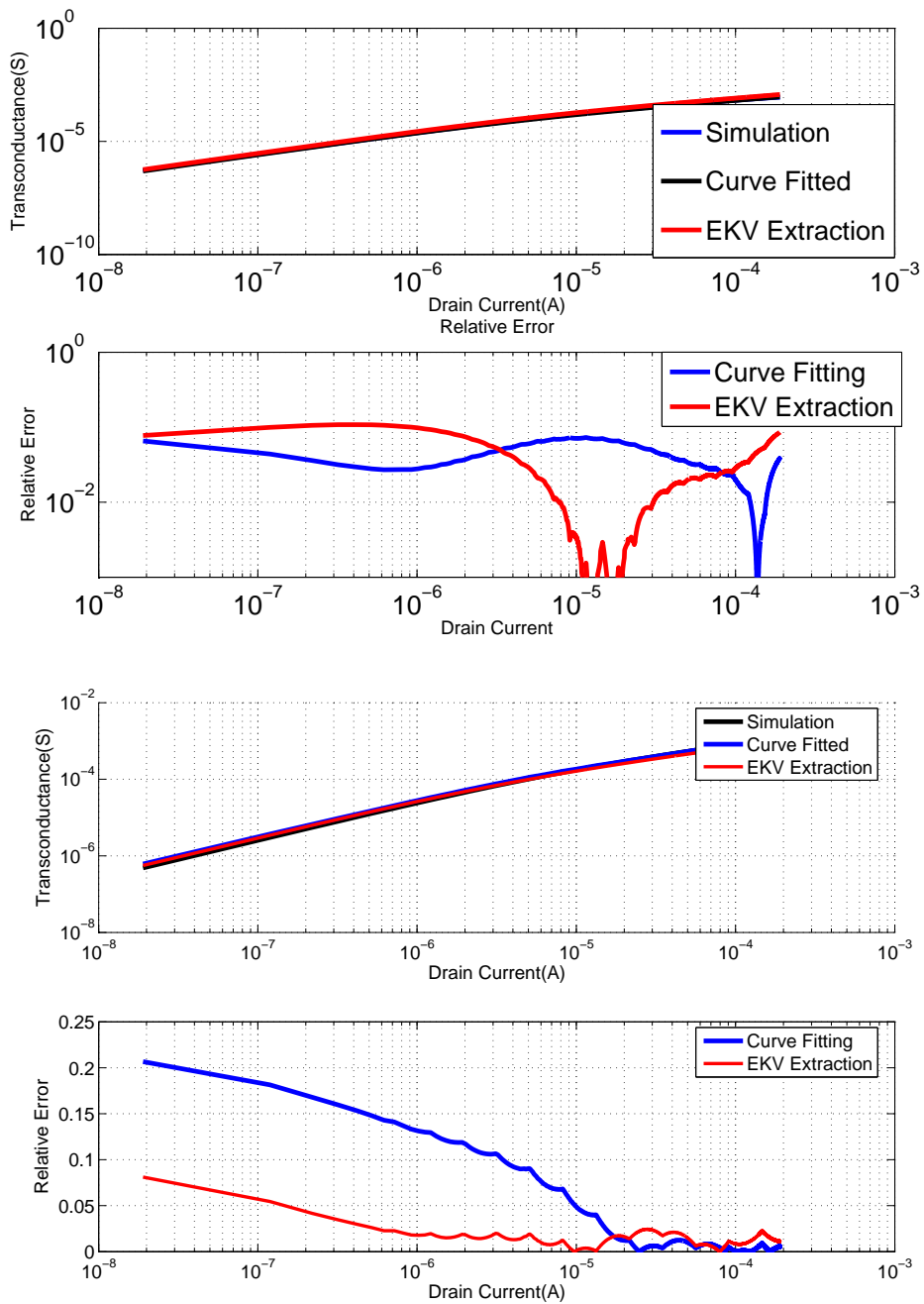


Figure 2.3: Model accuracy for transconductance: $G_m - I_d$ curves of a diode connected device for a short and a long channel device.

by defining a new normalization current I_0^{Cap} , to be determined through curve fitting and used only for capacitance calculations. To extract C_{gs} a diode connected device was simulated for $I_d = 10\mu A, 1 \leq W/L \leq 1000$. The rough results are shown in figures 2.4. Especially for longer channel lengths, two linear regions can be distinguished in the plot of C_{gs} versus W at fixed bias current. In the strong inversion region $C_{gs} \approx \frac{2}{3}C_{ox}W \cdot L$; in the weak inversion region instead $C_{gs} \approx C_{ol}W$. Since usually $C_{ol} \ll \frac{2C_{ox}L}{3}$ using the strong inversion equations to estimate capacitance can result in very pessimistic predictions. In the moderate inversion region, the overlap and intrinsic capacitance values are comparable, and device models are typically inaccurate. Using this extra fit parameter allows to improve the agreement can be to 15%. Table 2.2 summarizes the results from curve fitting of the capacitance curve. The adopted model allows us to combine

Polarity	L	n	I_0	C_{ol}	C_{ox}
$N(CFT)$	$.1\mu$	1.5	$.2\mu A$	$3.4e - 10$	$17e - 3$
$N(CFT)$	1μ	1.5	$.12\mu A$	$5.6e - 10$	$17e - 3$
$P(CFT)$	$.1\mu$	1.5	$.6\mu A$	$3.1e - 10$	$17e - 3$
$P(CFT)$	1μ	1.5	$.25\mu A$	$5.3e - 10$	$17e - 3$

Table 2.2: MOSFET model capacitance model extracted from simulation and curve fitting

information on transconductance and capacitance to estimate the transition frequency $f_T = \frac{g_m}{2\pi C_{gs}}$ of a device with a 30% maximum error compared to BSIM. In fact, usually $f_t^{(1)} = \frac{g_m}{2\pi C_{gg}}$ is more relevant to circuit design than f_t . Since C_{gg} is not as bias point dependent as C_{gs} , this figure can be estimated with even better accuracy. Consider finally the intrinsic device gain $A_v = g_m/g_{ds}$. The definition of a physical model for A_v has remained elusive despite considerable amount of research effort. However, we found that a very simple expression can be used to fit the peak gain of a device as a function of channel length. This is shown in figure 2.6, which reports the simulated intrinsic transistor gain of an MOS device versus inversion coefficients for different channel lengths. As usual, the curves have been obtained by simulating a diode-connected device and extracting values of transconductance g_m and output conductance g_{ds} from a DC analysis. The plot

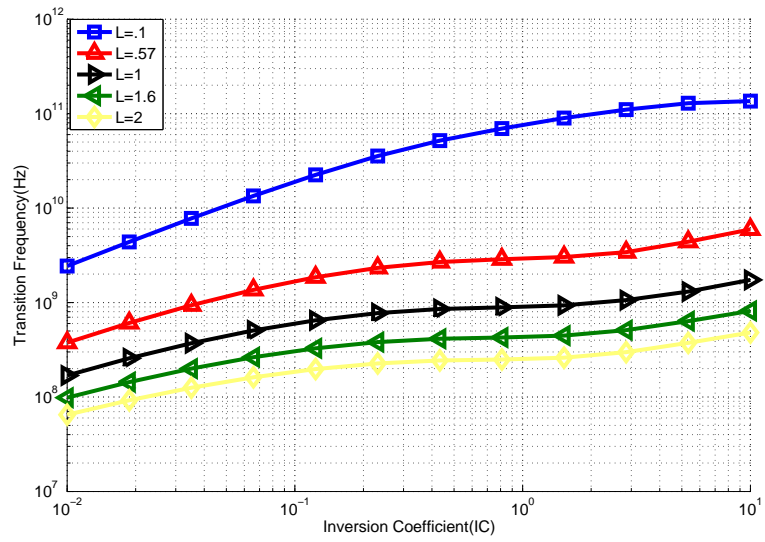
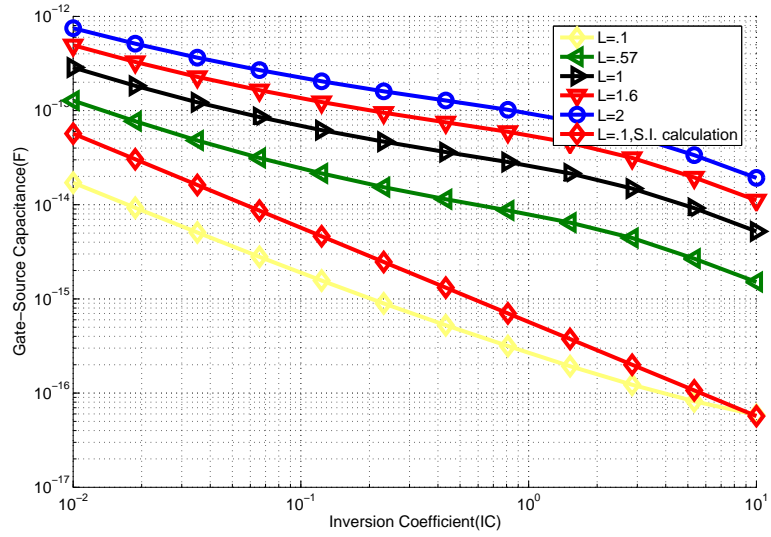


Figure 2.4: Simulated values of gate-source capacitance(left) and intrinsic speed f_t (right)

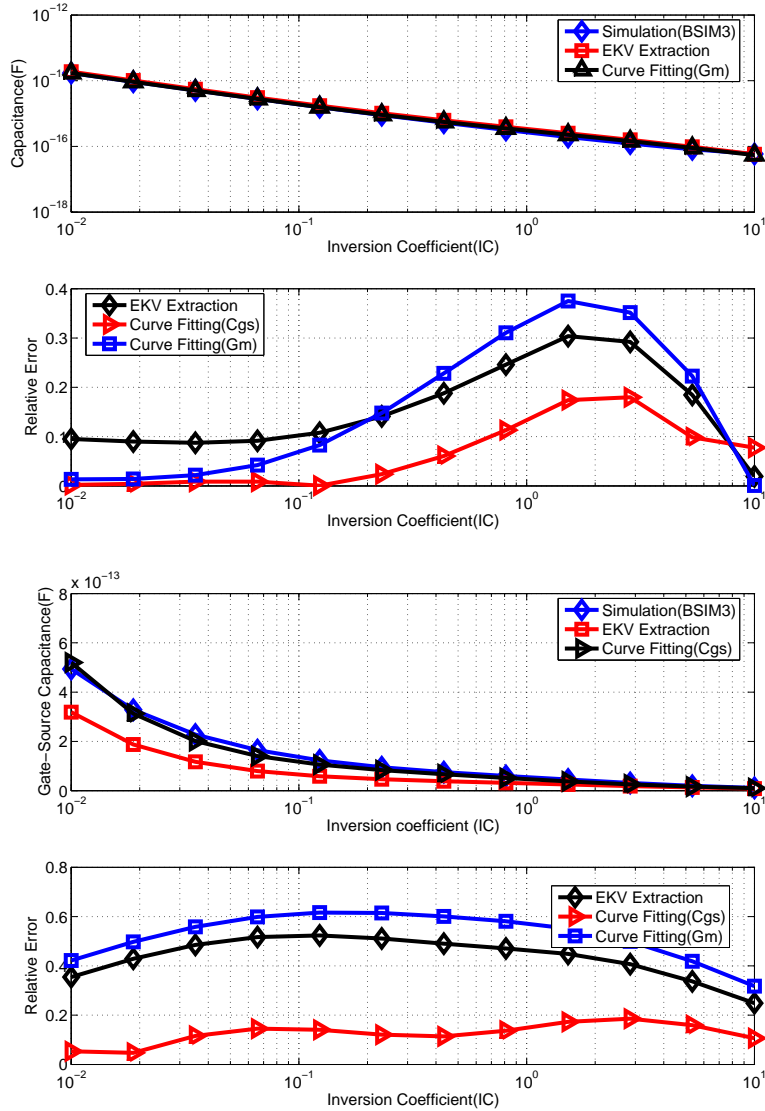


Figure 2.5: Model accuracy for capacitance: $C_{gs} - I_d$ curves of a diode connected device for a short ($L = .1\mu m$, left) and a long ($L = 1\mu m$, right) channel device.

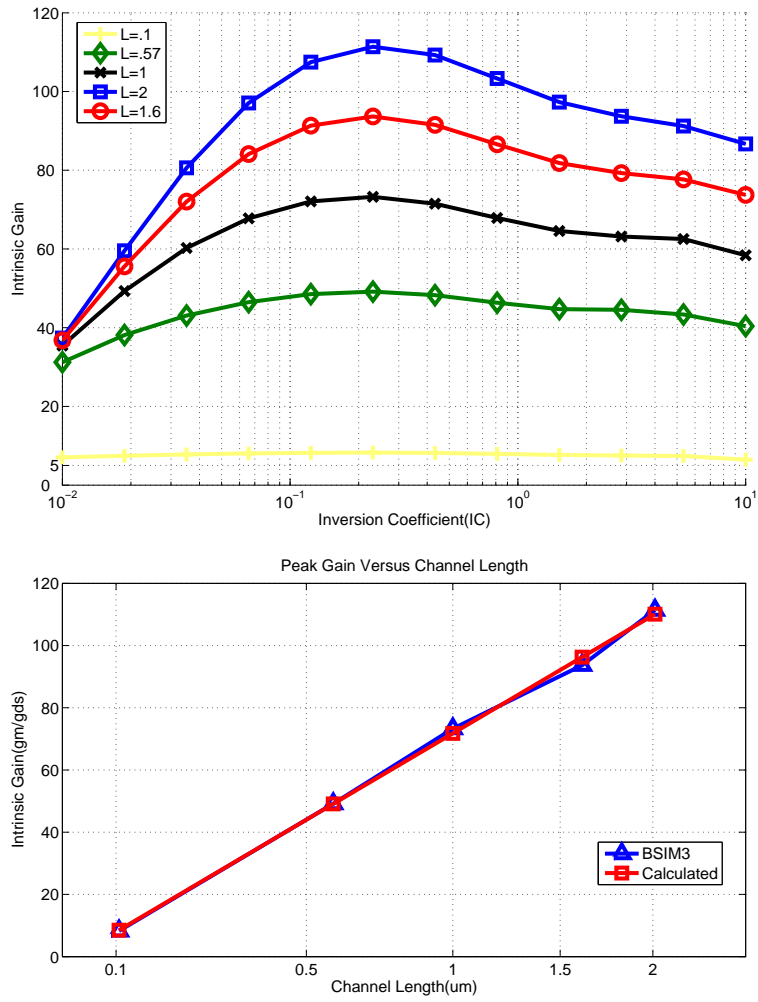


Figure 2.6: Simulated values of device intrinsic gain g_m/g_{gds} (left) and maximum intrinsic gain versus L(right)

in the right-half of figure 2.6 shows A_v^{Max} versus \sqrt{L} . We found that for this measurement setup and technology the expression $A_v^{Max} = -20.5 + 91.5\sqrt{L(\mu)}$ (L is the device channel length), approximates the peak gain with an accuracy better than 3% for N-type devices with L ranging between .1 and 2 microns.

2.1.3 Thermal Noise

For a long channel CMOS device the noise resistance is usually expressed as

$$R_{noise} = \frac{\gamma}{\alpha g_m} \quad (2.7)$$

. The parameter γ depends on the charge distribution and electric field magnitude in the channel, and it varies between 1/2 in weak inversion and 2/3 in strong inversion. For a short channel device, higher values of γ have been observed [15] in measurements. Such observation triggered a large amount of research in the device community with the aim to discover the physical origin of such increase in the noise floor. Interestingly enough, despite the high-field effects in the channel are often invoked to explain mismatch between measured and simulation data, such effects are supposed to appear only when the electric field in the channel approaches the critical field E_{crit} , which hardly happens even at the source end for bias voltage values used in analog design. Not a single work known to the author presents excess noise measurements for devices biased in weak or moderate inversion regions. As mostly non-minimum length devices were used in the design, the formula 2.7 was trusted, with $\gamma = 1/2, \alpha = 1$ for design purposes. It is the author's belief that, in the low-transverse-field operating conditions that are typical of analog design, this model is accurate not only for both short and long channel devices.

2.1.4 Gain-Speed Tradeoff

Using the results gathered so far, we can look at what kind of single stage gain can be realized at a given operating speed. This value, combined with an open loop gain specification determines the number of amplifying stages to be used, and therefore has very significant impact on power dissipation. In this respect, the most interesting parameter is $f_t^S = \frac{g_m}{2\pi C_{gs}} |_{IC=.1}$, the transition frequency of a device biased in weak inversion. Such a parameter has been already recognized in [16] as a fundamental milestone to distinguish specifications that can be implemented in a power-efficient manner. At $IC = .1$, one can confidently substitute $g_m = \frac{I_D}{nV_{TH}}$ and $C_{gs} = 10C_{ol}W = C_{ol}\frac{I_d}{I_0}L$. Also, by using equation $A_v = K_0 + K_1\sqrt{L}$, $L = (\frac{A_v - K_0}{K_1})^2$. Therefore

$$f_T^{(S)} = \frac{I_0}{20\pi \cdot C_{ol}nV_{th}} \left(\frac{K_1}{A_v - K_0} \right)^2 \quad (2.8)$$

A few numerical values are reported in table 2.3. Equation 2.8 and tab. 2.3

Minimum Gain(dB)	$f_t^{(S)}$
18	3GHz
33	.5GHz
37.2	.28GHz
39	.19GHz
40	.15GHz

Table 2.3: Transition frequency f_t achieved by a MOSFET biased at $IC=.1$ versus gain for NMOS in this process

show that increasing channel length only ensures marginal gains in maximum per-transistor amplification, while steadily decreasing the device intrinsic speed. However, minimum-sized devices are not a particularly good selection in low-voltage, low-speed environments, due to the extremely low intrinsic gain (and also high flicker noise). An optimal channel length should rather be chosen based on overall system specifications and selected amplifier topology.

2.2 Switches

Transistors used as switches are also a fundamental building block of every sampled-data system. The main limitations of such a building block have been recognized in the literature([17], [18]) to be finite(and input dependent) on resistance and charge injection. These limitations should be re-examined in the context of very low voltage operation. The main points addressed in these work are three:

1. The conventional transistor on-conductance model is inaccurate for very low supplies. A new model is proposed and evaluated to overcome this limitation
2. For low-supply, MHz-speed applications the main bottleneck is not on-resistance, but charge leakage. This effect is analyzed in detail in the following in terms of reduced I_{on}/I_{off} ratio and is ultimately a consequence of the fact the MHz-range applications are starting to get out the optimal operating range of fine line CMOS
3. In the low- V_{dd} regime, charge injection is substantially different than in the *high* - V_{dd} regime.

2.2.1 Switch Conductance Model

The on conductance of a device in the triode region, with a gate source voltage of V_{gs} is usually expressed as

$$g_{ds}^{(on)} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}(V_{in})) \quad V_{gs} \geq V_{th}$$

$$g_{ds} = 0 \quad V_{gs} \leq V_{th}$$

$$V_{gs} = V_{dd} - V_{in}$$

In implementations, switches are typically built using complementary topology, leading to $g_{on} = g_{on}^N + g_{on}^P$. In this case, equation 2.9 predicts $g_{on} = 0$ when $V_{dd} \leq V_{th}^N + V_{th}^P$. This conclusion is incorrect. In fact, as confirmed by 2.8, that

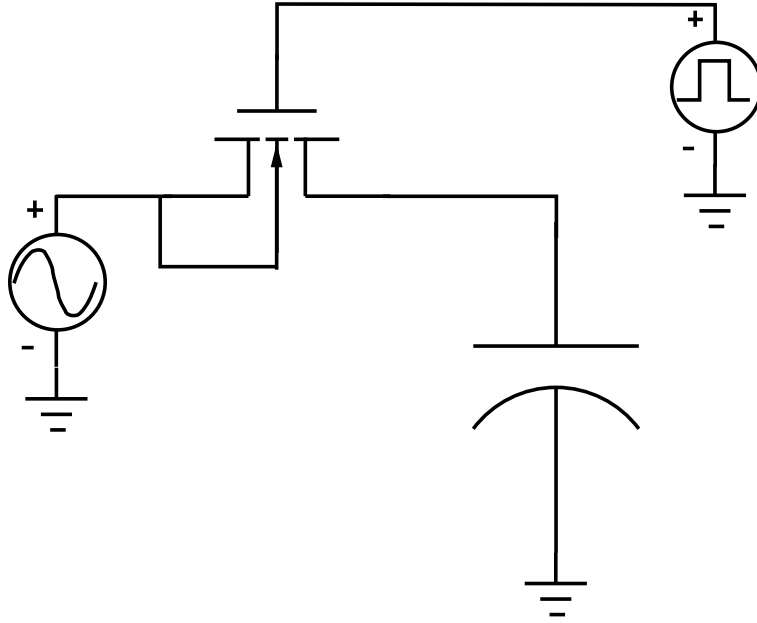


Figure 2.7: Simple NMOS switch

reports the on resistance of an elementary switch versus supply voltage and input voltage (expressed on the x axis as fraction of V_{dd}), for low values of V_{dd} the on resistance increases substantially but stays bounded.

Since, this work is primarily concerned with circuits operating in the $V_{dd} \leq V_{Th}^N + V_{th}^P$ regime a model of switch on-resistance for devices operating in sub-threshold is needed. In developing such a model, a fundamental choice is to opt for a device-physics based approach or for a curve-fitting based approach. In the interest of time, we opted for the second option, using an interpolation function to smoothen the transition between weak and strong inversion operation. We therefore need to derive a model for $g_{on}(V_{gs}, W, L)$, with special emphasis on the region $V_{gs} \leq V_{th}$. In order to simplify the task, we make the key observations that for $V_d = V_s$, assuming perfectly conducting gate electrodes, the charge distribution in the channel of an MOS transistor will be uniform across length and (neglecting edge effects) width. That is $Q_{ch}(x, y) = q \cdot N_{ch}(0, 0) = Q_{ch}(0, 0)$. Given that one can always express conductance as $g(x) = \frac{\mu_n N_{ch}}{\Delta X}$, the problem of calculating resistance is equivalent of that of finding an expression for the channel charge of an MOS device, so that modeling charge injection and modeling on-resistance are

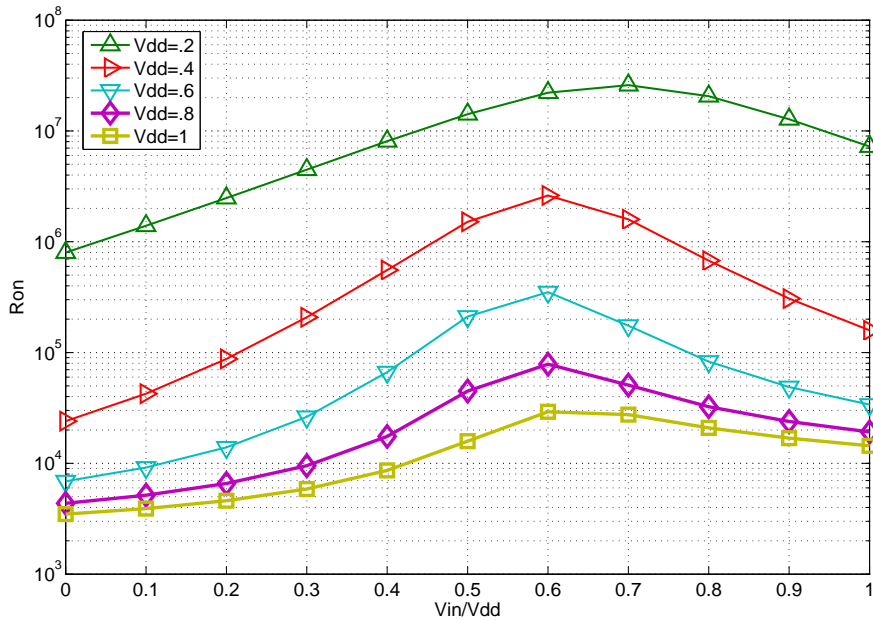


Figure 2.8: Sampling switch on resistance versus power supply and normalized input voltage

closely related tasks. The asymptotic requirements of an interpolation $f(V_{gs}, V_{th})$ for triode devices are readily derived. For high V_{gs} , $f \approx V_{gs} - V_{th}$ should hold. For $V_{gs} \ll V_{th}$ on the other hand, $f \approx \exp(\frac{V_{gs}-V_{th}}{nV_t})$. This constraints are met by the function 2.9

$$g_{on}(V_{gs}, V_t, W, L) = \frac{W}{L} K_1 \log(1 + e^{\frac{V_{gs}-V_{th}}{nV_t}}) \quad (2.9)$$

Where $n = 1.5$, $V_{th} = 26mV$, while k_1 was determined through curve fitting. This model guarantees an accuracy better than 25% on the range of $V_{dd} = .2V$ to $V_{dd} = 1V$ (See 4.6).

2.2.2 Charge Injection

In order to keep device resistance (and hence settling time) constant when reducing supply voltage, device width has to be increased. Potentially, this could increase charge injection. A closer look reveals that absolute value of charge injected by

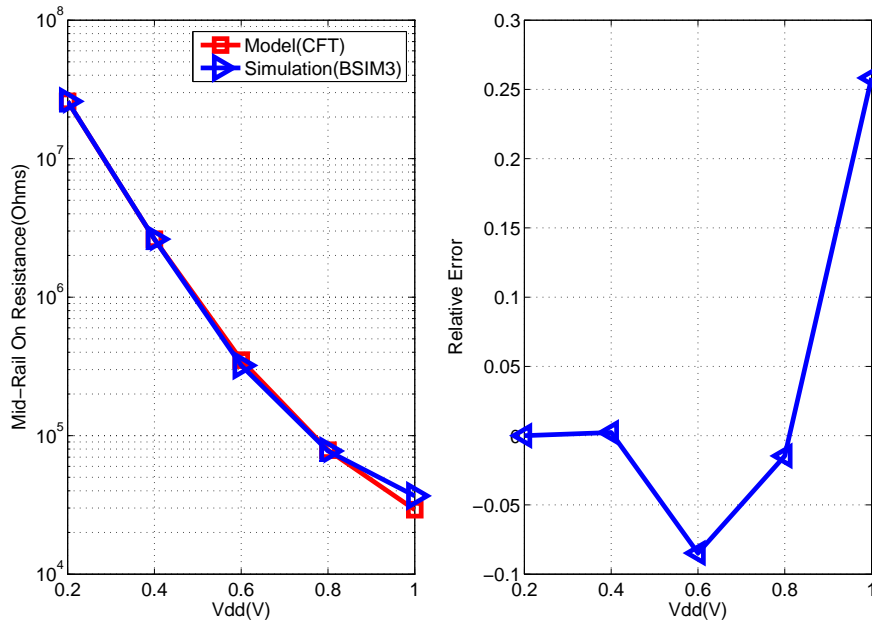


Figure 2.9: Sampling switch on resistance versus power supply and normalized input voltage

the switch is constant, while its dependence on the input is changed. Consider the device in figure 2.7, which has been purposely drawn with the bulk connected to the source, so that no body effect is present. For $V_{dd} = 1V$, the charge in the channel is well approximated by $Q = C_{ox}(V_{dd} - V_{th})$. When V_{dd} is reduced to $V_{dd}^{(2)}$, this charge per unit width is also reduced to $Q^{(2)} = Q \cdot \frac{f(V_{dd}^{(2)}, V_{th})}{f(1, V_{th})}$. Given that on-resistance is reduced by the same amount, the product $W/L \cdot Q$ should also stay constant, so that the total charge in the channel should be constant. However, the dependence of the charge in the channel on the voltage to be switched is different. In the extreme case of $V_{dd} \approx V_{th}$, $Q \propto e^{\frac{V_{gs} - V_{th}}{nV_t}}$. Therefore distortion due to charge injection is expected to increase for scaled supplies.

2.2.3 Charge Leakage

CMOS switch off resistance does not (to first order) depend on the supply voltage, while it does depend on the device width. This means while the voltage is scaled

from $V_{dd}^{(1)}$ to $V_{dd}^{(2)}$, and width is increased in order to keep R_{on} constant, R_{off} is roughly decreased by a factor of $\frac{f(V_{dd}^{(2)}, V_{th})}{f(V_{dd}^{(1)}, V_{th})}$. R_{on}/R_{off} ratio is therefore increase by the same amount. This effect, combined with the signal-dependent nature of R_{off} , creates large distortion at low supply values.

2.2.4 Sampling distortion simulations

Summarizing, we have individuated three mechanisms leading to degraded sampling linearity at low-supply. First, the increased sensitivity of resistance to voltage typical of subthreshold region results in higher R_{max}/R_{min} ratio when, for a given V_{dd} , V_{in} is varied. Second, the channel charge injected by the switch bears a strongly nonlinear relation to the gate-source voltage. This results into higher signal dependent charge injection even in the absence of body effect. Third, degraded R_{on}/R_{off} ratio leads to signal dependent leakage. All of these effects are simultaneously present, although we expect their relative contributions to be different in different contexts. Intuitively, charge injection and signal dependent on-resistance should be significant for relatively high-speeds, while charge loss should limit low speed designs. To isolate these effects in simulation, three different instances of the sampling switch are used (See figure 2.10). The first is a plain transmission gate switch, acting as a single ended passive sample and hold. In the second instance, an AHDL component operating as a switch with very small on-resistance and very high off resistance is added in series with the complementary device. This switch is opened slightly before the transistor-based switch, to suppress charge injection and charge leakage errors. Third, an ideally bootstrapped switch (such that $V_{gs} = V_{dd}/2$ for both devices independently of V_{in}) is used to isolate the charge leakage contribution. Using this configuration, three different cases were evaluated. First, we focus on the low-speed case, by designing an 8-bit linear sampling switch at $V_{dd} = 1V$. The sampling capacitance is set to $C_s = 1pF$, while the clock has duty cycle $\delta = .125^2$, and frequency $F_s = 1MHz$.

²Typical of a Successive Approximation ADC

To achieve 8-bits settling the on resistance of the switch should be such that

$$R \leq \frac{\delta}{8 \log(2) F_s C_s} \approx 10 K\Omega \quad (2.10)$$

at mid-rail. In fact, a minimum sized switch with $W_n = .12\mu$, $W_p = .36\mu$, $L_p = L_n = .1\mu$ has $R_{on} = 6.6K\Omega$. Table 2.4 reports the switches designed at reduced supply, along with the simulated R_{on} and R_{off} value. At $V_{dd} = 1V$, the simulated HD3 is 56dB, compliant with the 8-bits specification. In figure 2.11, the third order harmonic distortion of the switch in setup 1 is reported, together with those of switches 2(no charge injection, bootstrapped on resistance) and 3(no charge leakage) are reported.

V_{dd}	Device Width $[\mu]$	$R_{on}K\Omega$	$R_{off}(M\Omega)$
1	.1	6.62	80
.8	.13	10.3	60
.6	.6	10.5	45
.5	1.4	10	19.3
.4	3.6	10	7
.3	10.8	10	2

Table 2.4: On and Off resistance of low-speed switch design

Clearly, while both the nonlinearity due to input dependent on-resistance and that due to input-dependent off resistance increase with reduced voltage, the second is dominant in this setting. This is an optimistic picture, as process and temperature variations have not been considered. When these effects are taken into account, wider devices are necessary to achieve low-on resistance in the slow corner, low-temperature corner. This results in a further increased off conductance on the fast,high-temperature case, leading to higher distortion.

As expected, the breakdown is different when the speed is increased. If the same simulation setup is used to repeat the analysis for $F_s = 10MHz$, $\delta = .5$, as well as for $F_s = 100MHz$, $\delta = .5$, the results shown in Fig.2.12 are found. The target on resistances for 8-bits linearity driving a 1pF load in these cases are respectively 8.4 and .84 $K\Omega$. Figure 2.12 reports the simulated performance, which is clearly always limited by nonlinear resistance.

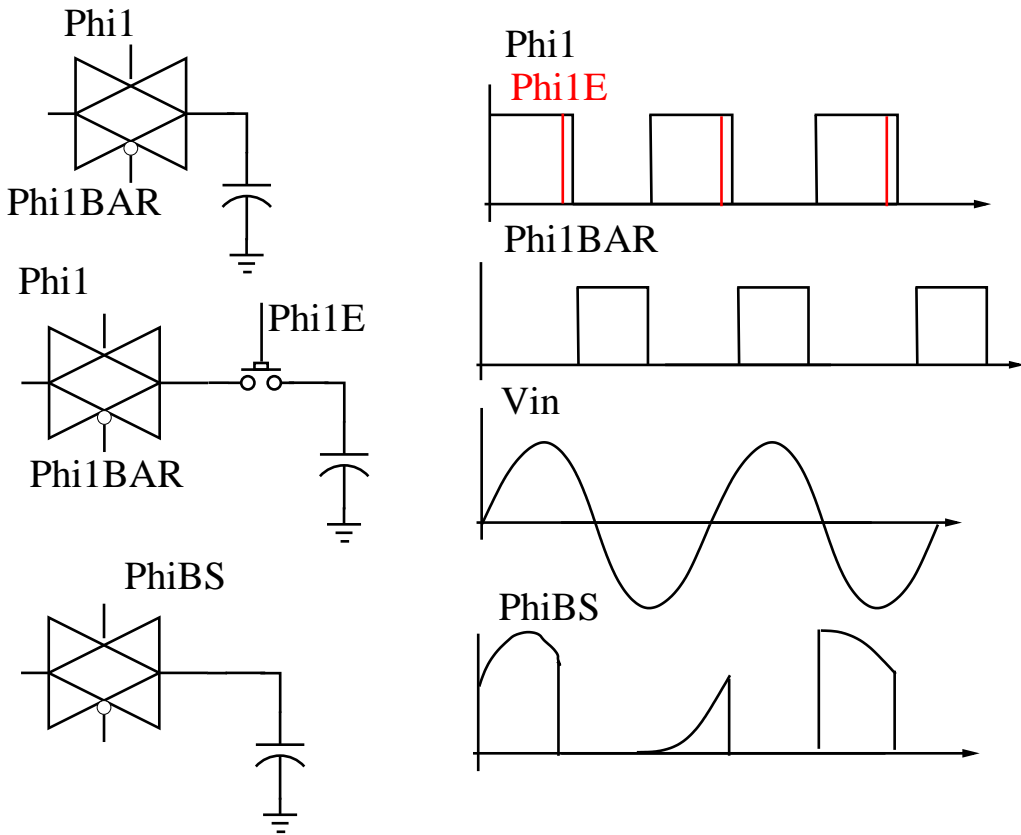


Figure 2.10: Simulation setup for the separation of sampling distortion contributions. From the top, conventional switch, configuration with series ideal switch for charge injection and charge leakage suppression, configuration with bootstrapped clock for signal dependent on-resistance and charge injection suppression

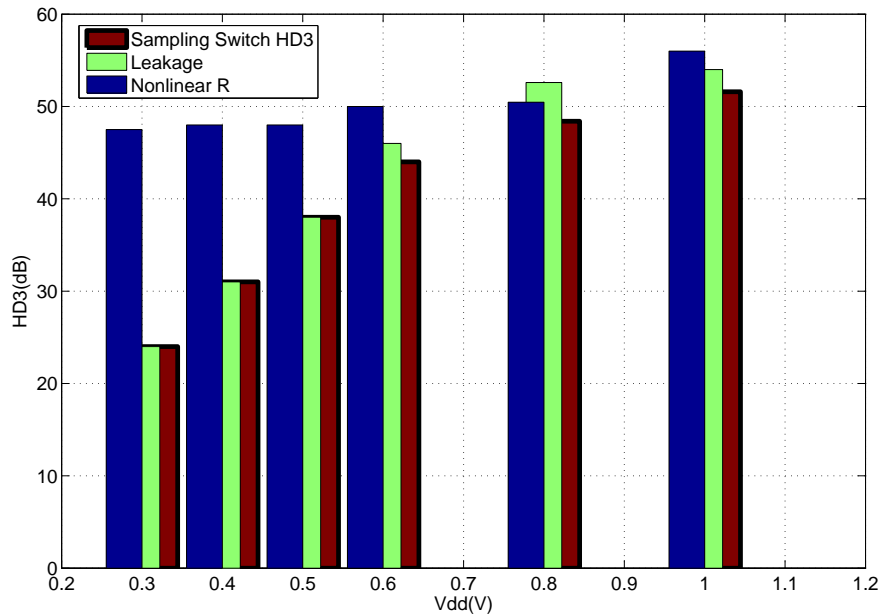


Figure 2.11: Contributions of charge leakage and nonlinear on-resistance to sampling switch nonlinearity

Discussion

Subthreshold conduction drastically limits the performance of low-speed charge based circuits. It is very interesting to notice how while 2.8 indicates an upper limit on the operating frequency where operational amplifiers can be designed in a power-efficient fashion, charge leakage dictates a lower-limit on the operating frequency. While charge leakage has been reported before [19] as a limitation to the performance of S/H amplifiers, in [19] the operating frequency was a few Hz; while the combination of technology and voltage scaling raise the bar to a few MHz. This result goes a long way in describing the effects of scaling.

In a different perspective, this result is quite similar to what is stated in [20], where the energy optimal V_{dd} of an FFT processor is studied. In both cases, subthreshold conduction discriminates what is *Slow* in the given process.

We also found that switch nonlinear resistance appears to consistently contribute a larger fraction of the total distortion than what the charge injection does. Accurate

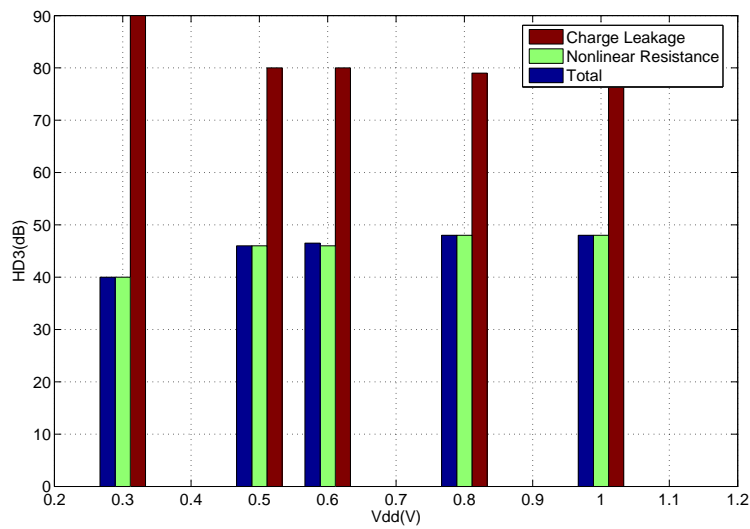
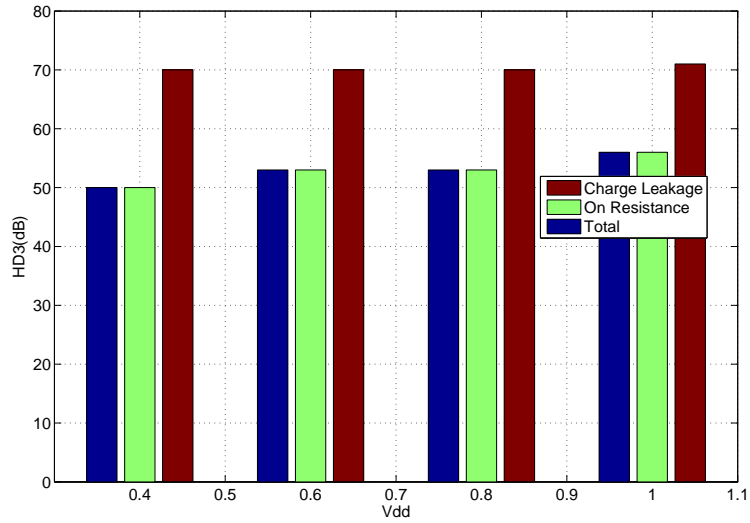


Figure 2.12: Simulated contributions to sampling switch nonlinearity for $F_s = 10\text{ MHz}$ (left)and $F_s = 100\text{ MHz}$ (right)

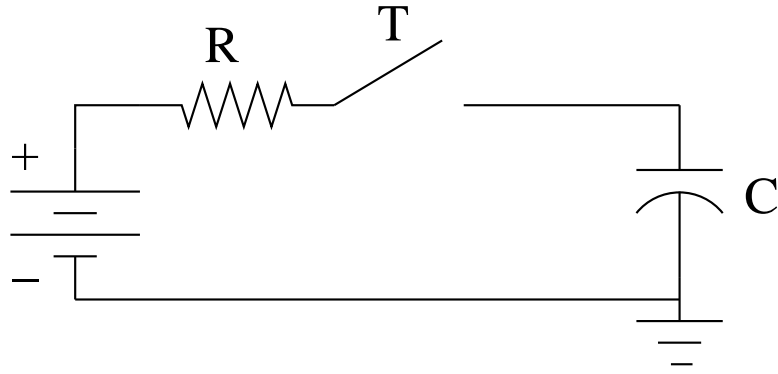


Figure 2.13: Idealized Sampling circuit

analytical modeling or measurements might give more confidence on the validity of this point, given that simulated results for charge injection are traditionally regarded as dubious.

Finally, note that the traditional view of NMOS being *faster* devices, or better switches has to be revised in the *low* – V_{DD} regime. For the process at hand the NMOS have a slightly higher threshold, which dominates the higher mobility effect for low values of V_{dd} . Due to this effect, low voltage transmission gate switches (See Chapter 5), sized for operating at 0.5 V have wider NMOS than PMOS devices.

2.3 Circuit design limitations

2.3.1 Thermal Noise

Consider the circuit shown in figure 2.13. It is known [21] that the variance of the noise sampled on the capacitor C is $V_n^2 = KT/C$. In a real switched capacitor circuit, noise from the active circuitry adds to the sheer sampling noise, so that in reality

$$V_n^2 = \frac{FKT}{C_s} \quad (2.11)$$

where the noise factor F depends on amplifier topology and sizing. For a given dynamic range specification, equation 2.11 can be used to calculate the minimum sampling capacitor size to be used by putting $V_n^2 \leq \frac{V_{sw}^2}{10^{DR/10}}$, or

$$C \geq \frac{F \cdot 10^{DR/10}}{V_{sw}^2} KT \quad (2.12)$$

. Not depending on any fabrication parameter, thermal noise is unanimously recognized the most fundamental limitation in analog circuit design. As a result, equation 2.12 has been used as the basis of more than one paper on analog voltage scaling ([22], [23]). In such works, the argument flows as follows: first, it is assumed that $V_{sw} = f(V_{dd})$ where f is a monotonically nondecreasing function. Given an SNR specification, and the value of the noise factor F , one can derive the capacitor size C_s . Power dissipation is then estimated making assumptions on the type of amplifier used, and the type of settling. For example, assume $f(V_{dd}) = V_{dd}$. In this case, if $P_d \propto V_{sw} V_{dd} C_L$ (slew-rate limited design), Eq. 2.13 holds

$$P_d \propto F \cdot 10^{DR/10} KT \quad (2.13)$$

. Therefore, power dissipation of slew-limited design should be to first order constant when the supply is scaled. For analog circuits that are not slew-rate limited, power dissipation is not proportional to the swing, so that the term V_{sw} would drop out of equation 2.13, leaving $P_d \propto \frac{1}{V_{dd}}$. These predictions have traditionally been disproved by experimental results for several reasons. First, supply scaling is usually accompanied by feature size scaling, and traditionally the increased baseline speed of new technologies provides gains that offsets the losses due to swing reduction. Second, these results assume that circuit is limited by thermal noise, and power consumption by that of operational amplifiers. Converter architectures that do not employ operational amplifiers are not included in this analysis, and are good candidates to have better scaling potential.

2.3.2 Device mismatch

Mismatch amongst active or passive components limits the performance of most low-resolution signal processing systems, including A/D converters. Active device mismatch is mainly determined by fluctuations in the threshold voltage of transistors, due to manufacturing tolerances. At the circuit level, it causes input referred offset in comparators and amplifiers. Flash converters are well known to be limited by offset in their comparators. Performance of current steering DACs is also limited by active device mismatch.

Passive device mismatch limits amongst others, resistive division D/A converters and capacitive division D/A converters, and all those data conversion systems that use these as building blocks. Errors due to capacitive mismatch can be written as $V_{err} = V_{dd} \frac{\Delta C}{C}$, and therefore scale with the supply. Accordingly, the size of passives, as dictated by mismatch constraints, is independent of the operating supply V_{dd} . This is remarked in figure 2.14, which also shows how, for a wide range of values of V_{dd} , matching limitations are way more stringent than noise limitations, or there is a waste of noise. As long as the supply voltage value is in this range, in virtue of the independence of switched capacitance on voltage C , power dissipation improves with decreasing supply.

2.3.3 Operational amplifier scaling

We now review operational amplifier design in a scaled V_{dd} environment in a quantitative manner. The factors limiting op-amp power dissipation can be summarized in three categories, settling constraints, gain constraints and stability constraints. These constraints are summarized in the following.

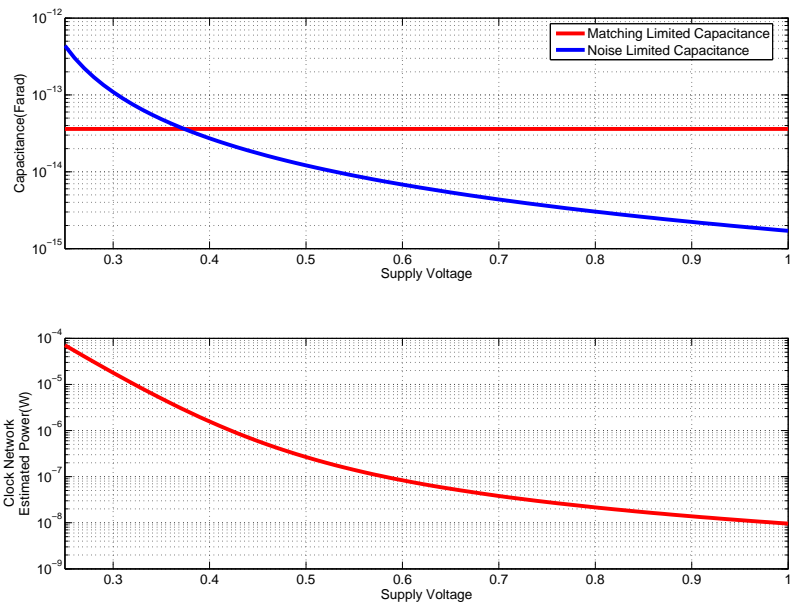


Figure 2.14: Minimum sampling capacitor size as derived from 8-bits noise and matching constraints

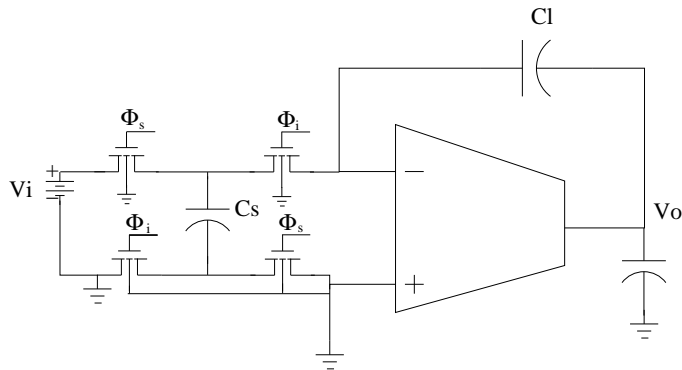


Figure 2.15: Example Switched Capacitor Integrator

Settling constraints I:Slewing

Consider the circuit shown in figure 2.15. The step response of such a circuit can be roughly divided into two sections, a slewing portion due to finite current drive ability of the operational amplifier, and a linear portion due to linear single(or multiple) pole settling. During the linear settling phase, $V_o(t) = V_o^* + (V_o(\infty) - V_o(t^*)) (1 - \exp(-(t - t^*)/\tau))$, with $\tau = \frac{C_L^{eff}}{G_m}$, with C_L^{eff} being the effective load at the output of the amplifier, equal to $C_L + (C_p + C_s)F$. C_s is the sampling capacitance, C_p the amplifier input parasitic capacitance, and $F = \frac{C_I}{C_s + C_p + C_I}$. Due to linear nature of the equations, the single pole settling portion is not influenced, to first order, by supply scaling. The slewing portion is however strongly dependent on it. We assume that during the slewing period, the current is limited to the value I_{slew} , so that $SR = \frac{I_{slew}}{C_L^{eff}}$. The end of the slewing period is the instant t^* such that $SR = \frac{\partial V_o^{(lin)}}{\partial t} = \frac{V_o(\infty) - V_o(t^*)}{\tau}$, or

$$t^* = \frac{(1 + \chi)V_{dd}C_L^{(eff)}}{I_{slew}} \quad (2.14)$$

χ is the charge sharing factor satisfying

$$\begin{aligned} G_{cl} &= \frac{C_s}{C_I} \\ a &= \frac{C_L}{C_s} \\ b &= \frac{C_p}{C_s} \\ \chi &= \frac{1}{1 + a(1 + G_{cl} + bG_{cl}) + b} \end{aligned} \quad (2.15)$$

. Downscaling of V_{dd} reduces the slewing fraction of the settling, at the expense of increased linear settling [24], irrespective of I_{slew} . This fact, combined with reduced I_{on}/I_{off} ratio, favors class A amplifiers over class AB ones. We'll therefore limit considerations in this paragraph designs of the former type. If a specified slew-rate SR^* is required, the slewing current should be larger than $SR \cdot C_L^{Eff} = \frac{V_{sw}}{t_{slew}} C_L^{Eff}$. This value of current depends linearly on the supply, so that if one estimates power dissipation finds:

$$P_d^{Slew} \propto \frac{V_{dd}}{f(V_{dd})} \quad (2.16)$$

which shows less pronounced dependence on V_{dd} than the equivalent for the settling-limited regime.

Settling constraints II: Linear settling

For a single pole amplifier, assuming the settling error is to be less than ϵ_d , one finds

$$\tau \leq \frac{-1}{2T_{clk} \log(\epsilon_d)} \quad (2.17)$$

$$\tau = \frac{1}{F \cdot UGB} \quad (2.18)$$

$$UGB = \frac{Gm}{C_{Leff}} \quad (2.19)$$

which can be solved for Gm giving

$$Gm \geq -\frac{2C_{Leff}}{F \cdot T_{clk}} \log(\epsilon_d) \quad (2.20)$$

Finally, one can estimate the power dissipation as

$$P_d^{(2)} \geq \frac{2Gm}{Gm_{eff}} V_{dd} = -2 \frac{2C_L}{F \cdot T_{clk}} \log(\epsilon_d) \frac{V_{dd}}{Gm_{eff}} \quad (2.21)$$

Stability constraints

Another set of limitations comes from stability considerations. In order to guarantee good phase margin, non dominant poles ω_{nd} in the amplifier response should be at least twice as large as the amplifier unity gain bandwidth UGF. For a large class of amplifier topologies, the lowest-frequency non dominant pole can be written as $\omega_{nd} = K\omega_T$ with K a topology dependent constant. Amplifier stability therefore trades off with per-transistor gain and speed. Given a speed and gain requirement, Table 2.3 can be used for every fixed amplifier topology to derive the necessary channel length and number of stages.

Intuitively, as the bandwidth increases, higher inversion coefficients and shorter

channels lengths have to be used, resulting in lower per transistor gain and therefore higher number number of stages. As the number of stages is increased, increasingly complex compensation techniques have to be applied, which typically result in increased power dissipation.

Comparison of different topologies

Since the final goal of this section is to determine what are guidelines for the design of operational amplifiers at low supply voltage, we compared quantitatively different class A amplifier topologies. The comparison is structured as follows. First, we introduce a reference ideal amplifier and a set of parameters to characterize different amplifier topologies in a compact way.

As reference class A amplifier, we choose an ideal component with noise resistance $1/G_m$, output swing $V_{sw} = V_{dd}$, and pure single pulse response. The transconductance efficiency is assumed to be 25, so that $I_{slew} = I_{dc} = 2G_m/25$. A real amplifier will be described by the set of parameters below:

- Noise factor $F = G_m \cdot R_n$ where G_m is the transconductance and R_n the equivalent noise resistance.

In low-voltage designs, we can assume that all transistors are biased sub-threshold(to maximize swing), so that the noise factor F is equal to the sum performed over all the devices contributing to total noise of bias current normalized to the input device bias current. No reduction in effective noise resistance through biasing is possible, as the price paid in terms of swing is too high in these conditions. This implies that simple structures are better suited for low-voltage, low-power design.

- Output swing V_{sw} .

Under the same assumption stated before of all devices operating subthreshold, the output swing is well approximated by 2.22:

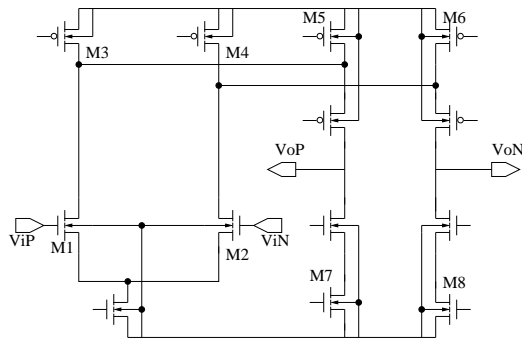
$$f(V_{dd}) = V_{dd} - n \cdot 120m - b \cdot 45m \quad (2.22)$$

being n the number of transistors stacked in the output stage and b is one if the amplifier has a tail current source, 0 otherwise. For example, an output stage with n stacked transistors, where n is assumed to be even, has $n/2$ transistors stacked between the output and V_{dd} and $n/2$ between the output and ground. The output can therefore swing between $V_o^{(Max)} = V_{dd} - n/2 \cdot 120mV$ and $V_o^{(Min)} = n/2 \cdot 120mV$, so that $V_{sw}^{PD} = V_{dd} - n \cdot 120mV$. If the output stage includes a current source, as in the case of telescopic amplifiers or of a standard differential pair, the output is assumed to be able to swing as low as $n/2 \cdot 120mV + 90mV$ and the swing is reduced to $V_{sw}^{FD} = V_{dd} - n \cdot 120mV - 45mV$.

- Power Factor P , equal to the ratio of total DC current drawn from the supply to DC current contributing to transconductance. Power factors close to 1 are desirable for low power.
- Non-dominant pole frequency ω^* , expressed as a fraction of device transition frequency. Topologies with higher ω^*/ω_T allow the use of longer channel devices, and hence provide higher per-transistor gain. This improves power efficiency

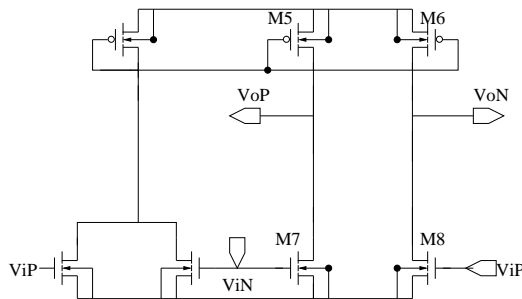
Example I: Folded Cascode Amplifier

For a folded cascode amplifier (shown in figure 2.16, the swing in the upward direction is limited by the PMOS current sources to $V_{dd} - 240m$. The downward limit for the swing is given by $240mV$, enforced by the folding devices and the current source load of the first stage. The contribution of the first stage to the total noise has been pessimistically assumed to be 2. The contribution of the folding stage to the total noise is given by the ratio of the current in the folding stage to the current in the transconducting stage. In general, this ratio will range between .5 and 1. It is therefore limited by the condition on the ω_T of the folding devices. These devices introduce a non dominant pole at $\omega_T^F = \frac{G_m^F(1+1/n)}{C_{gg}+C_{sb}^F} \approx \omega_T^F/4$ (The superscript is for Folding), which for stability reasons should be $\sigma \approx 2$ times higher than the unity gain bandwidth of the op-amp. In general, this ratio will



F	3 - 4
V_{sw}	$V_{dd} - 480mV$
P	2
ω^*	$\frac{\omega_T^F}{4}$

Figure 2.16: Summary of power analysis of Folded Cascode Amplifier



F	2
V_{sw}	$V_{dd} - 240mV$
P	$1 + \frac{1}{2B}$
ω^*	$\frac{\omega_T^{FCMC}}{4(B+1)}$

Figure 2.17: Summary of power analysis of pseudo-differential amplifier

range between .5 and 1, so that the total noise factor evaluates to 3 or 4. The power factor P equals respectively 1.5 or 2.

Example II: Pseudo-Differential common-source amplifier

A pseudo-differential common source amplifier with PMOS input and feedforward common-mode cancellation circuit is shown in figure 2.17. In this case, only two transistors are stacked between V_{dd} and ground so that $V_{sw} = V_{dd} - 240mV$ and $F=2$. The speed limitation comes from the common mode cancellation circuit, which is readily shown to have a pole in $\omega^* = \frac{\omega_T^{FCMC}}{8(B+1)}$.

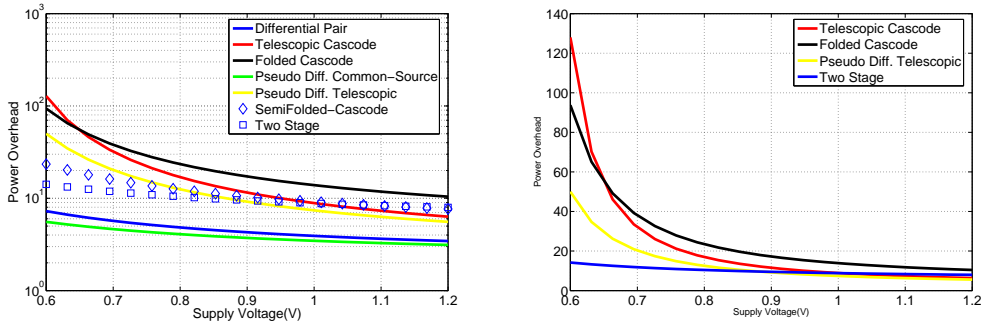


Figure 2.18: Power Dissipation scaling for different amplifier topologies operating in the settling limited regime

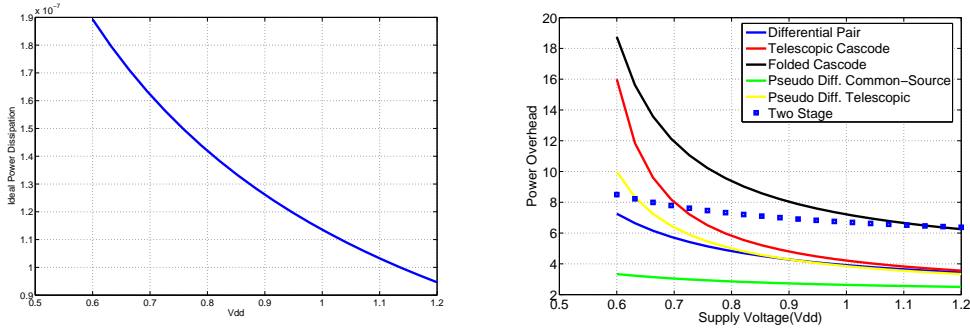


Figure 2.19: Power Dissipation scaling for different amplifier topologies operating in the slew-rate limited regime

Results

In the hypotheses of the analysis, relative power dissipation of any topology compared to the reference will be

$$\frac{25P \cdot FV_{dd}^2}{G_{mEff}V_{sw}^2} \quad (2.23)$$

for settling limited designs, and

$$\frac{25P \cdot FV_{dd}}{G_{mEff}V_{sw}} \quad (2.24)$$

for slew-rate limited designs. The results of the analysis are shown in figure 2.18 for settling limited designs and in figure 2.19 for slewing-limited designs. We see that in any circumstance, the simplest topologies, differential pair amplifiers and pseudo-differential amplifiers, provide the best power efficiency. Note that even though if the supply were to be scaled below .6V, two stage amplifiers would finally gain an advantage over differential pair amplifiers, these should still

be the preferred choice, as long as the low gain provided is tolerable.

If however only topologies capable of providing a gain of at least $(g_m r_o)^2$ are considered, two stage amplifiers appear the best choice in the settling limited regime for voltage less than about .9V, while a telescopic structure retains a superior efficiency for longer time in the slewing-limited regime. Also, while being outperformed by multistage amplifiers, telescopic structures retain better power efficiency than folded ones for power supply values as low as .65V due to the better power factor P.

Analysis Limitations and amplifier bias point optimization

The presented analysis did not take into account self loading effects. In real amplifier implementations, the parasitic input capacitance of the amplifier C_p degrades the feedback factor F, resulting in decreased power efficiency. This effect can be analyzed by using the simple 1-transistor amplifier in 2.20. For this amplifier, $F = \frac{C_f}{C_f + C_s + C_{gg}}$. For a given bias current, increasing the device width increases both G_m and C_{gg} , so that an optimal value of IC(or equivalently W) can be chosen. In this work, this task has been solved analytically by assuming $C_{gg} \approx W(LC_{ox} + C_{ol}) = \frac{W}{L}C_0$. If F is further assumed to be independent of C_{gg} , the resulting optimal inversion coefficient is given by equation 2.25.

$$b = F \frac{C_0 I_d}{(C_s + C_L) I_0}$$

$$IC_{opt} = b + 2\sqrt{b} \quad (2.25)$$

The price paid in settling speed for operating at an inversion level higher than the optimal one is modest for moderate misalignment. However, the price paid for operating at inversion level *lower* than the optimal is very high. This should therefore be avoided. The results for $C_f = 1.5pF$, $C_s = 500fF$, $C_L = 250fF$, $I_d = 10\mu A$ are shown in figure 2.21 for different values of device channel length. These curves have been obtained using a much more accurate numerical model that takes into account bias dependent C_{gs} , slewing and variable feedback factor F. Using this method, the predicted optimal inversion coefficient is .3 for $L = .35\mu m$ and

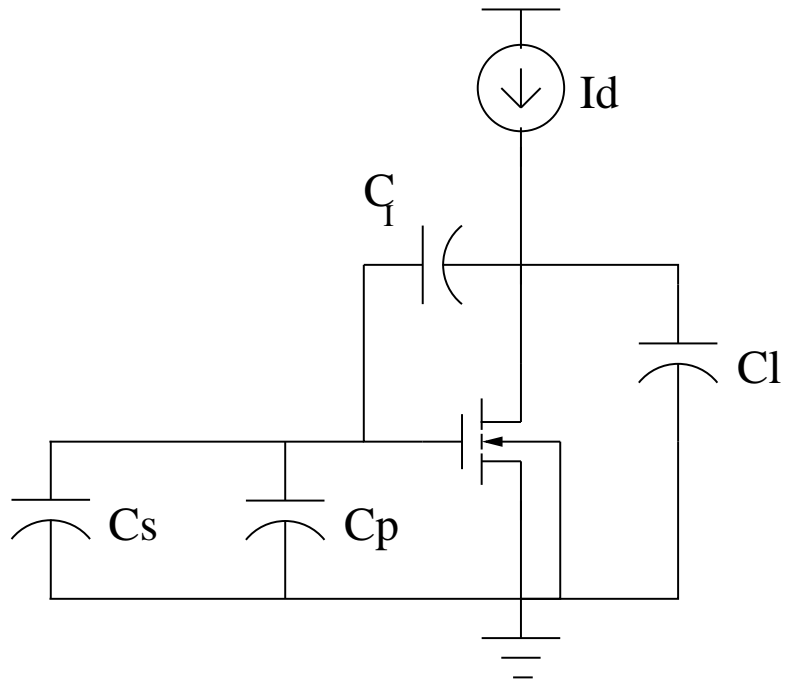


Figure 2.20: 1-transistor amplifier used for bias point optimization

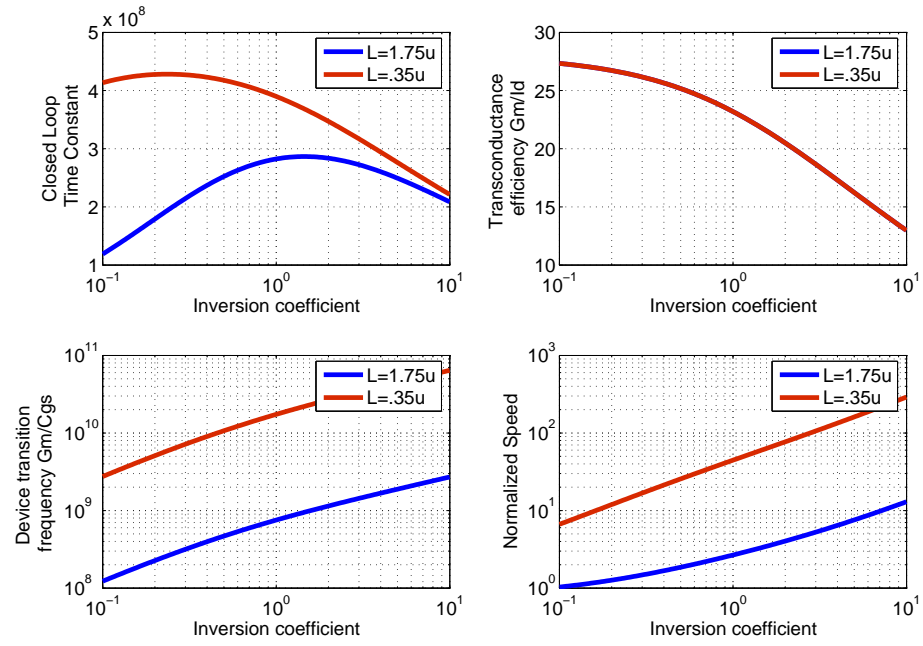


Figure 2.21: Optimal Inversion coefficient selection for a 1-transistor amplifier

1.5 for $L = 1.75\mu m$. Using formula 2.25, one finds respectively IC_{opt} to equal .38 and 2.1, which is reasonably close to the optimal value and shows that equation 2.25 can be used for amplifier sizing. In fact, it is interesting to observe that since for a given dynamic range the relative advantage of using a differential pair amplifier instead of two-stage amplifier is a factor of 3 or smaller, it is possible that the power reduction gained from being able to use smaller channel length devices will overcome this limitation. For instance, with reference to figure 2.21, for a sampling capacitor of 500fF, using a .35 μ device in the input stage instead of a 1.75 μ one results into a boost of 50% in the maximum settling speed, and in a 25% transconductance efficiency improvement. These effects combine for already 60% of the power advantage of the simpler stage. Multistage amplification should therefore be considered in the range of available options for low-power design at low supplies.

2.3.4 Other building blocks

Comparators

Comparators are quite resilient to voltage scaling. In principle, the minimum operating voltage for cross coupled latch-based comparator is that value such that the gain of a CMOS inverter operating under such a V_{dd} decreases below 1 and is on the order of 100mV. In practice this limit is hardly achievable for multiple reasons:

- Running digital logic at .1V is possible only if the logic is custom designed. This increases substantially design time and strongly limits speed. Also, .1V almost surely is also an inconvenient choice in terms of energy/operation([20])
- The design of any circuit other than an inverter will be challenging at such low voltage. Think for example of preamplifier and sampling switch design

- Offset specifications become challenging as the supply is reduced. For instance, achieving a $3 - \sigma$ offset at the 4 bit level requires, for $V_{dd} = .1V$ requires $\sigma(V_{io}) \leq \frac{V_{dd}}{3 \cdot 2^B} = 2mV$. This requires large devices and relatively high power dissipation

Nonetheless, comparators typically consume very little power when running at MHz speed, so that they do not constitute a particular worry. Furthermore, in chapter 3 we report experimental data showing correct operation of a comparator when $V_{dd} = .3V$, demonstrating that comparators are unlikely to constitute a problem in low-voltage designs.

Digital logic

Most converters require a certain amount of digital logic to perform operations such as bit-realignment in a pipeline architecture, sequencing in a SAR architecture or decimation in oversampling converters. The cost of such logic in terms of power is negligible in most applications, and very little consideration has been devoted to its evaluation. At the bare minimum, in order to perform decoding each comparator output needs to be sampled with a register. For B bit of resolution, B registers are necessary. From simulation, it was found that a standard-cell library flip-flop, when configured as a frequency divider by 2, is 60nW when the input frequency is 10MHz and $V_{dd} = .5V$. Although very small, this number becomes significant when the total budget is only a few microwatts. Furthermore, leakage power, which is poorly modeled and highly process dependent, typically contributes a large fraction of digital power so that making conservative design is a necessity. This is made clearer in Tab.2.5, where the number of FO4 registers that would contribute 10% of the power budget when running at .5V reported for different values of total power consumption. Although digital power can be reduced by using custom designed gates, keeping complexity as as possible low in the digital domain is clearly advisable.

Power budget	Number of registers
$1\mu W$	2
$10\mu W$	20
$1mW$	2000

Table 2.5: Equivalent number of digital gates for a power budget

Sampling operation and clock tree constraints

We have seen in a previous section how as V_{dd} is decreased, ensuring sampling linearity requires an increase in switch width. This not only makes the switch design challenging as discussed above, but also increases the load of the clock tree. Using equation 2.9, the width of the sampling devices can be selected, that yields the desired on-resistance value. From $C_{gg} \approx C_{ox}(W_n L_n + W_p L_p)$, the capacitive loading contributed by every sampling switch C_{sw} on the clock tree can be calculated, and from this, an optimal clock buffer can be designed. Called $F = \frac{\sum_i C_{sw}^{(i)}}{C_{ui}}$ (C_{ui} is the input capacitance of a unit inverter), the optimal tree has $K = \lceil \log(F) \rceil$ stages, and the power dissipation of the clock tree results expressed by:

$$P_d^{Tree} = C_u V_{dd}^2 (F - 1) / (1.7). \quad (2.26)$$

In figure 2.22, normalized power dissipation of the clock tree is shown versus supply voltage when the sampling switches are designed to settle with 8-bits accuracy on the worst case mid-rail input voltage and the capacitive load is fixed. As long as the supply voltage is significantly higher than the threshold voltage of the switches, the power in the clock network is reduced. This is because $F \propto \frac{1}{V_{dd} - V_t}$ so that $P_d \propto \frac{V_{dd}^2}{V_{dd} - V_t}$. As V_{dd} approaches V_{tn} however, the capacitance increases exponentially, so that power in the clock network increases dramatically. In the case in the example, the optimal supply voltage may not be calculated analytically, but it apparently is located around .5V. For values of V_{dd} below .5V, the power raises quickly, and starts to be significant over a $10\mu W$ budget. The situation is even worse in noise limited designs, where the capacitor sizes (and thus F) scale as $\frac{1}{V_{dd}^2}$, leading to much faster increase of the clock power. It is apparent from the figure that to keep the clock power below 10% of a $10\mu W$ budget, V_{dd} should in this case

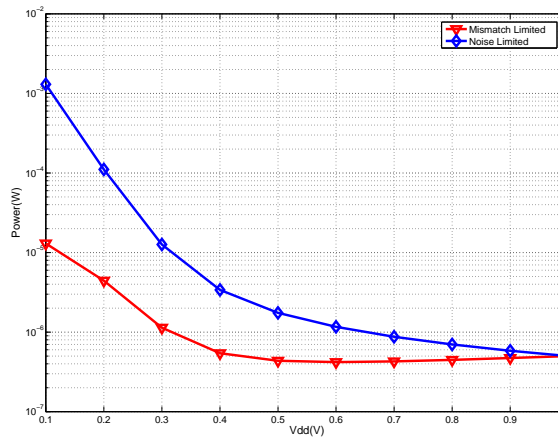


Figure 2.22: Power dissipation in the clock network when driving a constant capacitance (red) and when driving a capacitance proportional to the squared inverse of V_{dd} (blue, noise-limited scenario). The capacitance driven by the clock network is assumed equal to 100fF at 1V

be larger than .65 V.

2.4 Converter Architecture selection

In light of the considerations in chapter 2, the following guidelines have been derived

- A 100KS/s Nyquist converter could hardly be implemented in 90nm CMOS due to sampling switches charge leakage. The high speed and high leakage of the technology demand oversampling techniques to be used.
- Digital complexity should be minimized.
- The number of high gain stages should be minimized.

Architectures fulfilling these guidelines are recognized to be flash, successive approximation converters, and $\Sigma - \Delta$ converters⁽³⁾. Due to their fully parallel nature, Flash converters are immediately recognized to be inefficient compared to successive approximation ones when the sampling frequency is much lower than the device f_T . As this is definitely the case in this work, they are considered no further. A set of power estimation routines were implemented in MATLAB based on equations 2.26-2.21. Table 2.6 summarize this analysis, while table 2.7 presents a literature survey of recently published low-power analog to digital converters. For amplifier-based converters, such as pipelined ADC and $\Sigma - \Delta$, the power was assumed to be contributed by the clock network and the first OTA; for the successive approximation converter instead, it was assumed to be dominated by the comparator and the clock network. The estimated performance of the consid-

Architecture	Resolution	F_s	Est.Power	Est. Input Cap.	V_{dd}	FOM(pJ/conv)
SAR	8b	100KS/s	$.25\mu W$	1.28pF	1V	.009
SAR	6b	1.5MS/s	$.4\mu W$	320fF	.5V	.004
Pipelined	6b	1MS/s	$144\mu W$	50fF	1V	2.2
$\Sigma - \Delta$	12b	100KS/s	$12\mu W$	$65fF$.65V	.029
$\Sigma - \Delta$	14b	40KS/s	$147\mu W$	$220fF$	1V	.22
SAR	12b	100KS/s	$1.6\mu W$	$180pF$.5V	.004

Table 2.6: Comparison of low power ADC architectures(I):Estimated power and input capacitance

Reference(Arch.)	Resolution	F_s	Power	Input Cap.	V_{dd}	FOM(pJ/conv)
[25](SAR)	8b	100KS/s	$3\mu W$	3pF	1V	.24
[26]($\Sigma - \Delta$)	14b	40KS/s	$140\mu W$	$6pF$	1V	.22
[27](SAR)	12b	100KS/s	$25\mu W$	<i>n.r.</i>	1V	.165
[28](SAR)	12b	1MS/s	$15mW$	21pF	5V	3.6

Table 2.7: Comparison of low power ADC architectures(II):Literature Survey

³for the latter, the decimator will consume significant power. However, the large oversampling ratio in this case enables also other system-level advantages, such as alias and channel select filter complexity reduction

ered architectures matches that of published results to a reasonable degree. The capacitance estimate is however fairly inaccurate, and respectively optimistic for $\Sigma - \Delta$ modulators since only sampling noise is considered and quite pessimistic for high-resolution SAR converters since fully binary DAC architectures are always assumed.

Some conclusions can still be drawn. Pipelined converters appear less power efficient than both $\Sigma - \Delta$ and successive approximation converter, due to the tighter amplifier gain and settling constraints. SAR converters appear as ideal candidates for low-voltage, low power implementation when the resolution is limited to 6 or 8 bits; however, they suffer from increased input capacitance compared to $\Sigma - \Delta$ modulators. Although the estimated value in 2.6 for a 12b design is pessimistic as it assumes a straightforward binary weighted DAC implementation, the increased capacitance may still cause increased power dissipation and implementation area at the system level. Also, thanks to oversampling and to the absence of floating nodes, $\Sigma - \Delta$ converters present an inherent advantage in an environment with reduced R_{off}/R_{on} ratio. Finally, the estimated power of the SAR converters does not include digital power. As stated in a previous section and confirmed by [27], this power will be significant or even dominant with respect to the extremely low analog portion.

The architecture of choice for minimum power should therefore be a SAR for low or moderate resolution, while $\Sigma - \Delta$ for high resolution.

Chapter 3

Implementation I: a .5V, 6b, 1.5MS/s successive approximation converter

As a first proof of concept, a prototype 6b,1.5MS/s SAR converter was designed to operate from a .5V supply using 90nm CMOS.

3.1 Converter architecture

A building block diagram of the proposed SAR converter architecture is reported in figure 3.1. As the design of current steering DAC at 0.5V was thought to be a significant challenge, charge based processing was preferred, so that the feedback digital to analog conversion is realized through the binary weighted capacitor array C_p, C_n .

The input data is sampled by S_1 and S_2 on the top-plates of C_p and C_n during the sampling phase Φ_s . When Φ_s goes low, S_1 and S_2 open and the bit cycling phase begins. This phase consists of 7 periods of the decision clock Φ_f which acts as timing signal for comparator decisions and is provided through a dedicated pin. The digital logic operates in a synchronous fashion, clocked by a delayed version of the same signal, and applies feedback by controlling the bottom plates of C_p

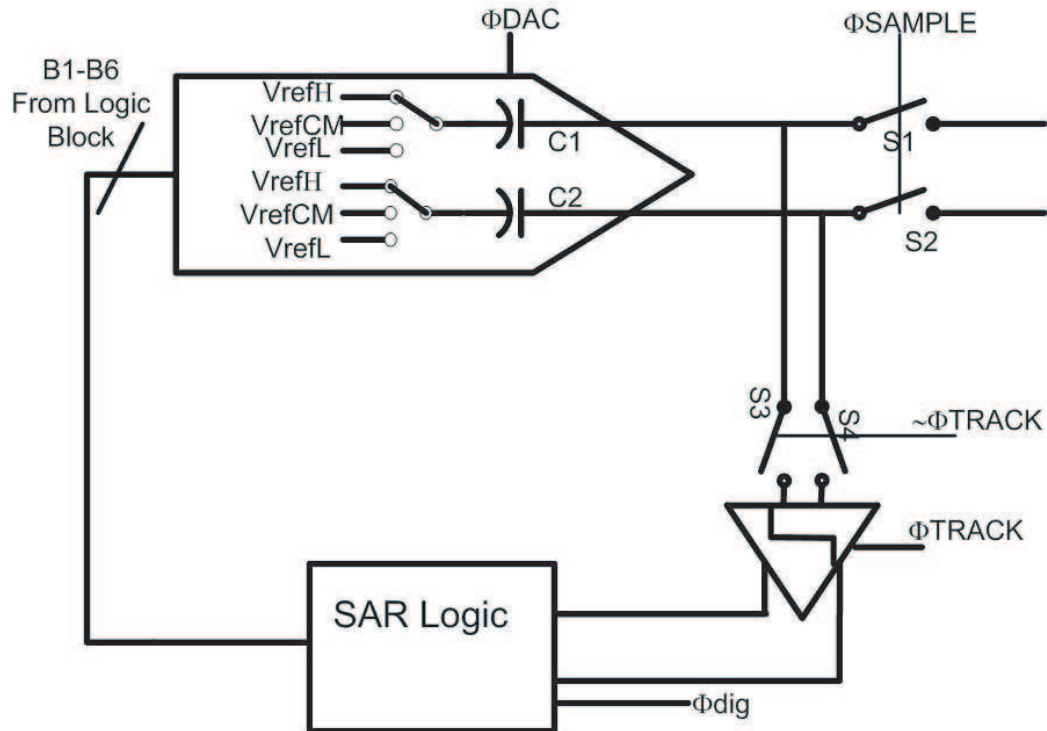


Figure 3.1: Converter architecture

and C_n . Notice that as explained in a following chapter, the digital to analog converter uses sign magnitude coding. Therefore, during the first clock cycle of the bit-cycling phase, the bottom plates of C_1 and C_2 are tied to $V_{dd}/2$, and the sign of the input is determined by the comparator decisions. During the following 5 cycles of the bit cycling phase, the absolute value of the input voltage is converted; one cycle is wasted.

3.2 Sampling Network design

To minimize power, a passive sample and hold is chosen. As discussed in Chapter 2, when bulk 90nm devices are used the frequency is low enough that switch linearity is easily achieved even at $V_{dd} = .5V$, while charge leakage is a concern. To reduce leakage, the sampling switches are realized using high- V_t (HVT) devices. Thanks to an additional implant, these devices have a threshold voltage

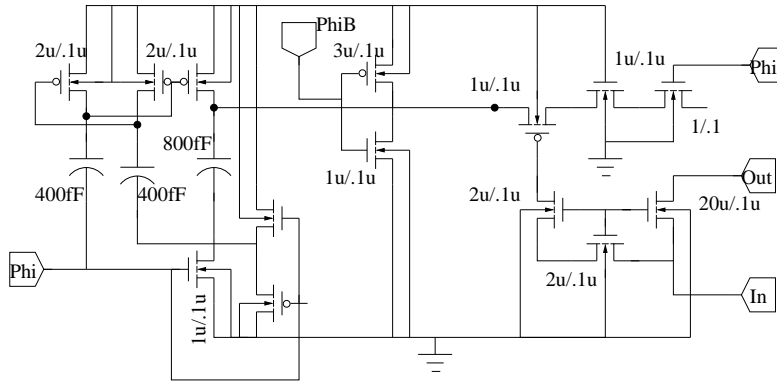


Figure 3.2: Annotated clock booster schematic

roughly 80mV higher than the standard V_t ones, which results in over an order of magnitude higher off-resistance. Due to the low-supply however, the minimum on-resistance of such devices also increases by the same amount, introducing memory effects in the sampling operation. To counteract this effect and ensure sampling linearity, the bootstrapped sampling switch introduced by Abo ([29]) is used. The schematic of the bootstrapped switch is reported in figure 3.2 along with device sizings. Capacitors used to store the charge necessary to generate the $2V_{dd}$ rail are realized with a high-density MIM layer to minimize area consumption; the bulk of M1 is grounded to save area and improve positive to negative side matching, as the resulting sampling distortion and signal dependent charge injection are not a concern at 6b-level.

3.3 Digital to Analog Converter

The digital to analog converter exploits sign-magnitude code and tri-level unit elements to reduce its total capacitance. The concept of tri-level elements is displayed in figure 3.3 for the case of a single element. Both the positive and the negative side capacitors can be connected to V_{dd}, V_{ss} or $V_{cm} = \frac{V_{dd}+V_{ss}}{2}$. Clearly, the configuration where C_p is tied to V_{dd} and C_n to V_{ss} encodes +1, while -1 is

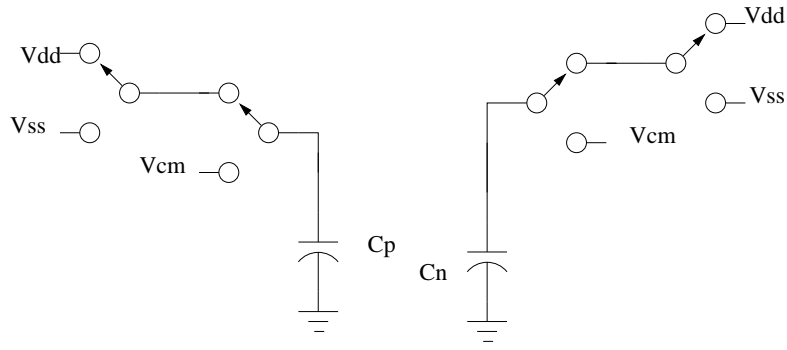


Figure 3.3: Unit element of a tri-level digital to analog converter

encoded is by the C_p, V_{ss}, C_n, V_{dd} pairs. Finally, 0 is realized by connecting both C_p and C_n to V_{cm} .

As proved in App.A, this architecture is advantageous in terms of linearity and total capacitance with respect to a two-complement counterpart. This advantage descends from the fact that the total number of capacitors necessary to realize a B-bits DAC using this approach is $2^{B-1} - 1$, half than for the two's complement counterpart. Consequently, the ratio of the variance of the peak INL to the variance of unit element mismatch is also halved(See Appendix A for derivation). Combining these two results we conclude that a four-fold reduction in total capacitance can be achieved for a given target resolution by using this technique.

Further reduction in the total capacitance can be reduced by choosing an appropriate capacitive layer. MIM capacitors offer the lowest capacitance per unit mismatch, and are therefore used in high-performance applications. From design equations however, we see that in order to obtain a $3 - \sigma$ INL better than .1 LSBs, a unit element variance σ^2 of 4.1e-3 is required(i.e. $\sigma = 6.5\%$). Even using a conservative approximation for the mismatch per unit area coefficient A_e , the capacitor area corresponding to this value of σ is smaller than the minimum capacitance value allowed by the design kit for the MIM layer. To keep unit capacitance as small as possible, we decided to use use M6-M5 capacitors¹. Due to the low density, a $5\mu m \mu m$ structure laid out using this layer has a capacitance of a few femtoFarads, but preserves matching properties comaprable to those of

¹Vertical parallel plate capacitors with plate distance equal to the inter-layer dielectric thickness

MIM. A conservative choice of $C_u = 10fF$ was made for the unit capacitor value to reduce the impact of fringing and similar edge effects on the array.

The layout of the capacitor array was realized by L.Wang of U.C. Berkeley. The switches driving the bottom plates are placed in close proximity of the array itself to minimize parasitics, and realized with standard V_{th} devices with $W = 1\mu$, $L = .1\mu$. A fully centroided structure was adopted, and a row of grounded dummies was placed around the active devices to avoid edge effects. As capacitor mismatch for this layer is determined by inter-layer dielectric thickness variations, dummy filling was added by hand and in a symmetrical fashion.

3.4 Comparator

The comparator shown in figure 3.4 and originally proposed in [30] was used. Devices with non-minimum channel length were employed to achieve an offset voltage lower than 1 LSB.

During the tracking phase, devices M3 and M4 operate as triode resistors, and constitute a load for the transconductors M1 and M2. For the given sizing, the bias current through M1 and M2 is determined by input common mode voltage and the device sizing and threshold voltage to be $I_{cm} = \frac{W_1}{L_1} I_0 \log \left(1 + \exp \left(\frac{V_{cm}^{(i)} - V_t}{2nV_{th}} \right) \right)^2 \approx .5\mu A$. The common mode voltage at nodes 3 and 4 during this phase therefore is $V_{cm}^{(3,4)} = V_{dd} - R_3 \cdot I_{cm} \approx .4$, and the differential gain during tracking is $A_{dm} = G_m^{(1)} R_3 = .5$.

During regeneration the voltage difference between nodes 3 and 4, $V_{3,4} = A_{dm} V_{in}$ is regenerated to the rails by the cross coupled pair M5-M8. Simulated waveforms of the comparator during overdrive recovery test ([31]) are shown in figure 3.5. Although this comparator has low power dissipation and can operate from a very low supply voltage, it generates a large amount kickback noise because of the poor isolation between input and output nodes. This is problematic in a successive approximation converter because the critical nodes are floating for the whole length of the conversion. To prevent kickback noise from disturbing the conversion, an additional set of switches is added in front of the comparator. These switches are

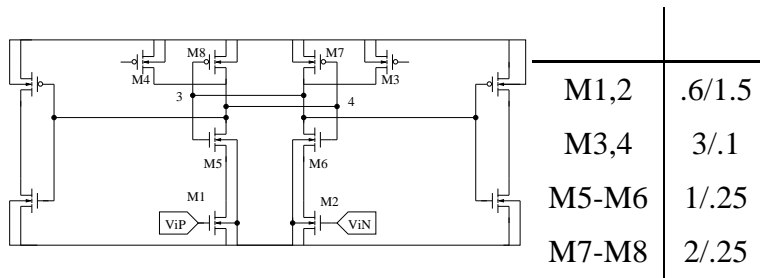


Figure 3.4: Comparator schematic and device sizing

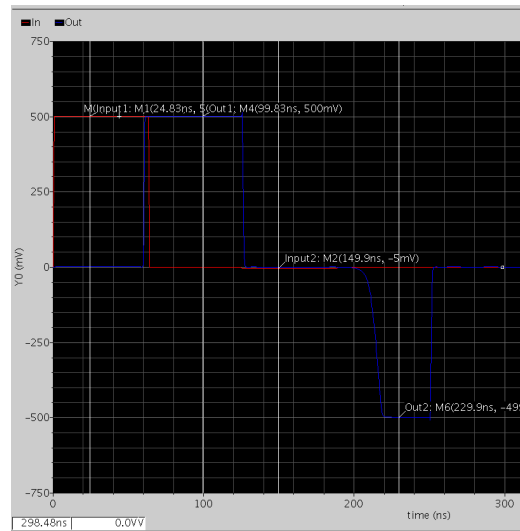


Figure 3.5: Simulated overdrive recovery test

closed during the tracking phase, and are opened immediately before the latching phase begins. The opening of these switches introduces a signal-dependent charge injection, which ultimately results in static and dynamic nonlinearity. This error has however been verified through simulation to be much less severe than that due to the kickback noise.

The layout of the comparator(except for the isolation switches) is shown in figure 3.6. A fully centroided structure is used to minimize systematic offset. The area of the comparator is $18\mu \times 16\mu$, and its simulated power consumption 625nW on the typical corner, and $1\mu\text{W}$ on the fast corner.

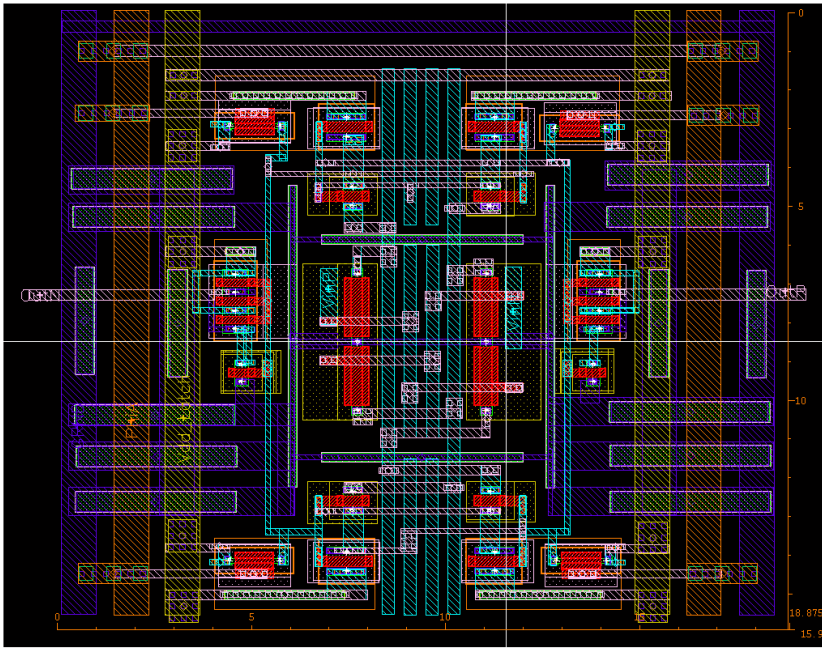


Figure 3.6: CAD Layout of the clocked comparator

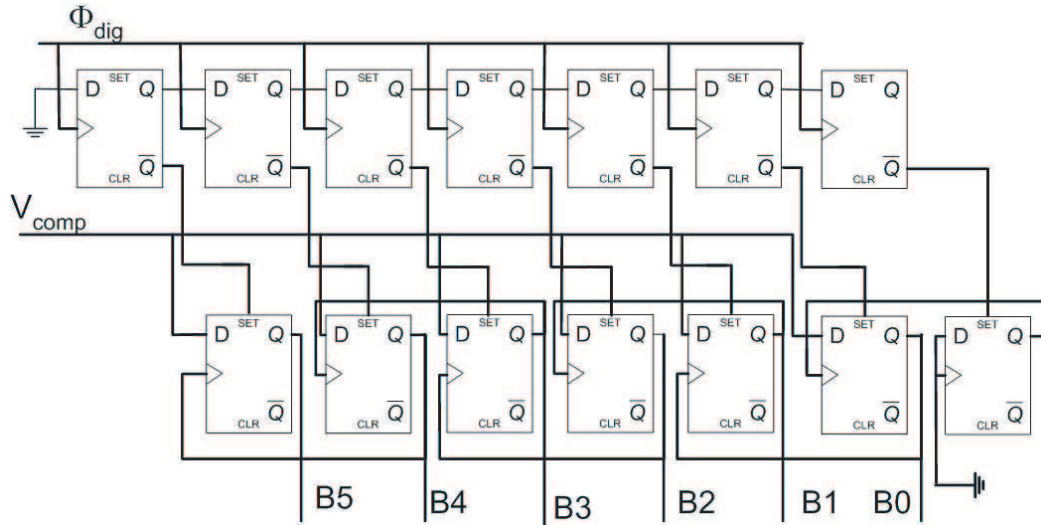


Figure 3.7: Schematic of the digital logic backend

3.5 Digital Logic

The digital logic was implemented using standard cell library gates. The architecture of the digital section is the same used in [25] and displayed in figure 3.7; it makes use of 2 shift registers to implement the successive approximation routine. The upper shift register is clocked synchronously by the fast clock Φ_f and is used as a sequencer, while the lower register is used to store the conversion value. When the reset signal arrives, the sequencer is reset in the 100000 condition. At every subsequent fast clock rising edge, the 1 value propagates along the sequencer, so that i clock cycles after the reset edge, it passes from the i -th position to the $i+1$ -th. This signal is fed to the set input of the $i+1$ -th flip-flop in the conversion register, and causes it to raise its output to 1. Finally, this output is used to clock the i -th flip-flop in the conversion register, that stores the current comparator decision. Because in the flip-flops used D input is disabled when the Set signal is high, a minimum delay has to be guaranteed between the instant when the set signal is deactivated and the arrival of the clock. To meet this constraint, a slow delay line generating 5nS of delay was inserted between the output of the $i+1$ -th register and the clock input of the i -th register.

Corner	Leakage	Dynamic	Total
TT	$1\mu W$	$1.2\mu W$	$2.2\mu W$
FFA	$2.3\mu W$	$1.2\mu W$	$3.56\mu W$
SSA	$.3\mu W$	$1.2\mu W$	$1.5\mu W$

Table 3.1: Simulated digital power dissipation at 1MS/s

This architecture relies on the ring structure to achieve a low-switching activity, and therefore low active power dissipation. However, the large number of registers used increases leakage current, which is a concern at low speed. Due to the low operating voltage and frequency, power dissipation of the digital logic was assumed to be negligible at design time. Therefore, no effort was done to reduce this contribution. In fact, the power dissipation of the digital section resulted significant in final system simulations and in measurements. Table 3.1 displays the simulated power dissipation figures, as well as the leakage versus active power breakdown, for different proces The power dissipation from the digital section is in the best case one and a half times higher than that from the comparator. Furthermore, a large fraction of this power is due to leakage, which is known to be poorly modeled and highly process dependent. This fraction of power could be lowered in several ways: first, logic could be restructured, and number of registers reduced to minimize leakage; second, custom, minimum sized logic gates could be used to decrease switching power. Finally, high-threshold devices could be employed instead of standard- V_t ones to further reduce standby power. Some of these techniques have been used in the second generation successive approximation converter described in chapter 5.

3.6 Measurement results

The chip was fabricated in a 90nm 7M2P CMOS process from ST microelectronics. The final top level layout is shown along with the die photograph in figure 3.8.

The total chip area(including padding) is $865\mu \times 730\mu$, while the core area is only

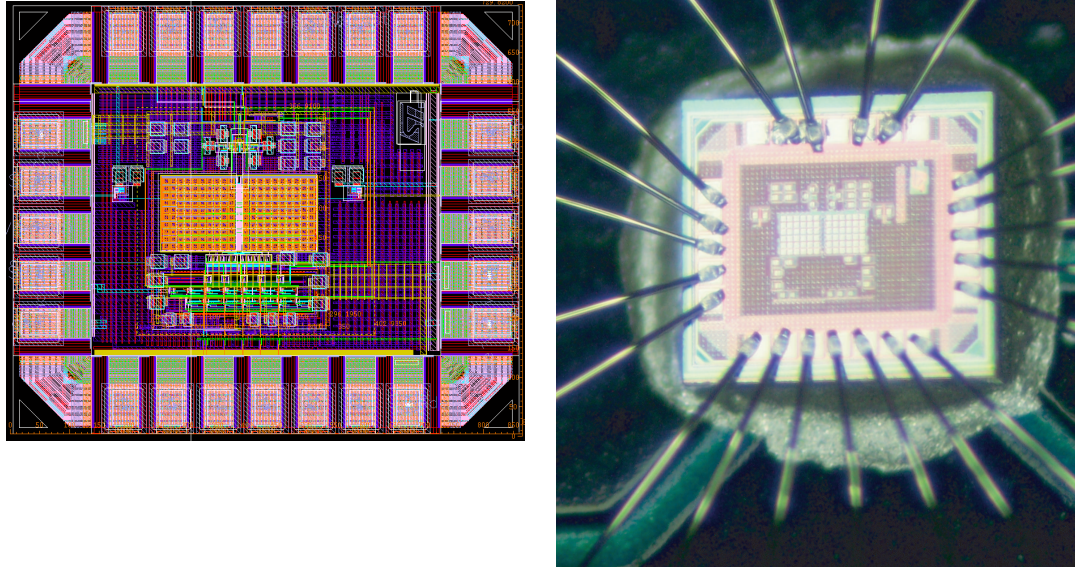


Figure 3.8: Layout capture(left) and chip microphotograph(right)

$300 \times 300\mu$, largely consumed by the capacitor array and the digital logic. Due to the small size, COB packaging was used for testing. 3 different samples were fully tested. The results are reported in figures 3.9-3.11, and summarized in table 3.2.

3.7 Performance

For FFT testing, a Rhode and Schwarz Signal Generator was used to generate a single-ended input voltage, that is converted to differential by an ADI 8138 part on the board. A logic analyzer is used for code read back and to provide both a fast and a slow(sampling) clock. For enhanced testability, the output code of the converter is not latched on the die, so that convergence of the successive approximation algorithm can be observed during testing. Timing of the read back consequently becomes critical. To overcome this problem, both the output bits and the clock are oversampled by the LSA, and the correct code is reconstructed

Performance Metric	Value
Voltage Supply	.5V
Input Range	.4V
Sampling Rate	1.5MS/s
Unit Capacitance	10fF
DNL	$\pm .4LSB$
INL	$\pm .4LSB$
ENOB	5.5 at Nyquist
ERB	2.5MHz
SFDR	43dB at $f_s = 1.5MS/s$ $f_{in} = 100KHz$
Power dissipation	$14\mu W$
Die Area	$.09mm^2$
Input Capacitance	200fF differential
Process	90nm 7M2P CMOS

Table 3.2: Performance Summary

Section	Sim.Powr	Measured Power
Analog	$2\mu W$	$2.5\mu W$
Digital(Leak)	$1\mu W$	$6\mu W$
Digital(Dynamic)	$1.2\mu W$	$3\mu W$

Table 3.3: Power dissipation breakdown

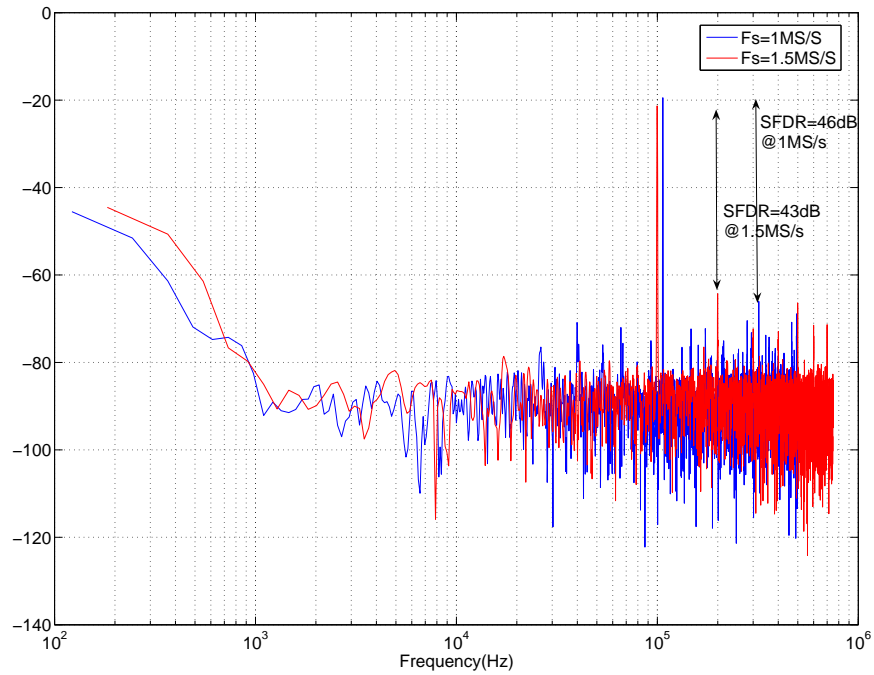
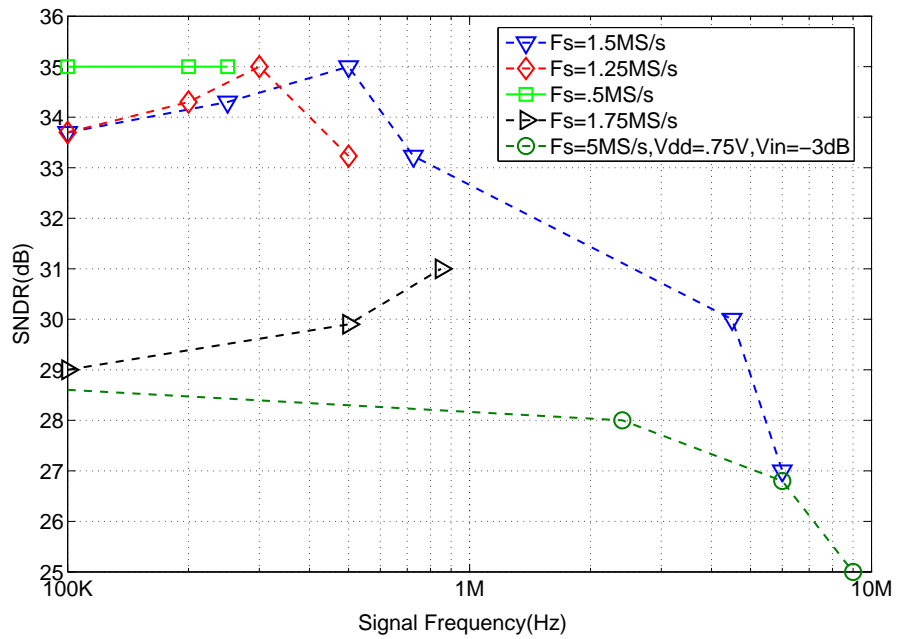


Figure 3.9: Dynamic Performance from FFT testing

in software by sampling each bit in its validity interval. FFT testing reveals that a peak SNDR of 34.5dB(5.5ENOB) is achieved for .4V zero-peak input at 1.5MS/s. When the sampling frequency is decreased, the peak SNDR stays constant or im-

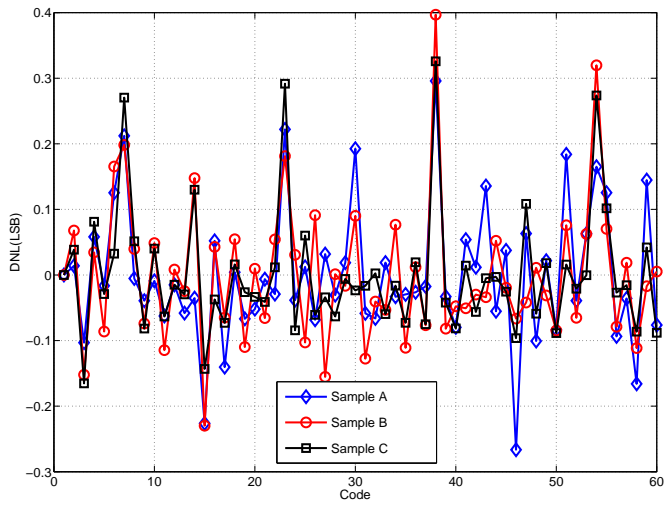
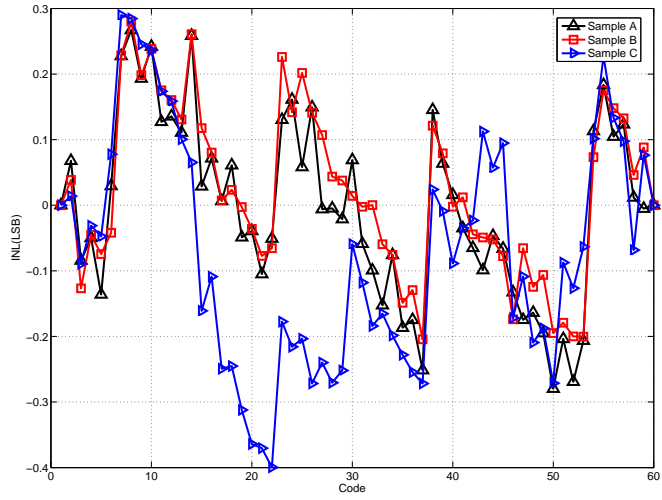


Figure 3.10: Static Linearity measured through histogram testing

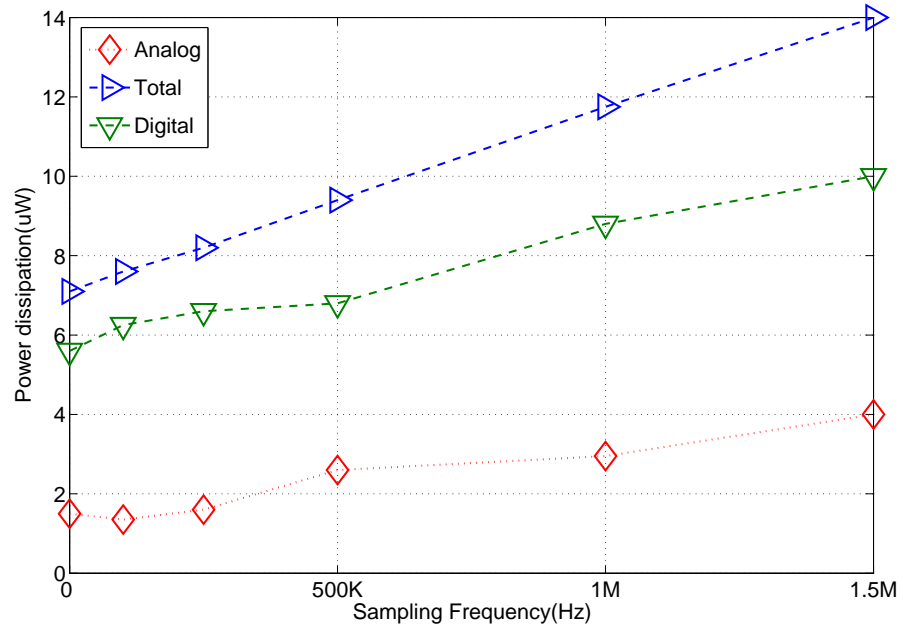
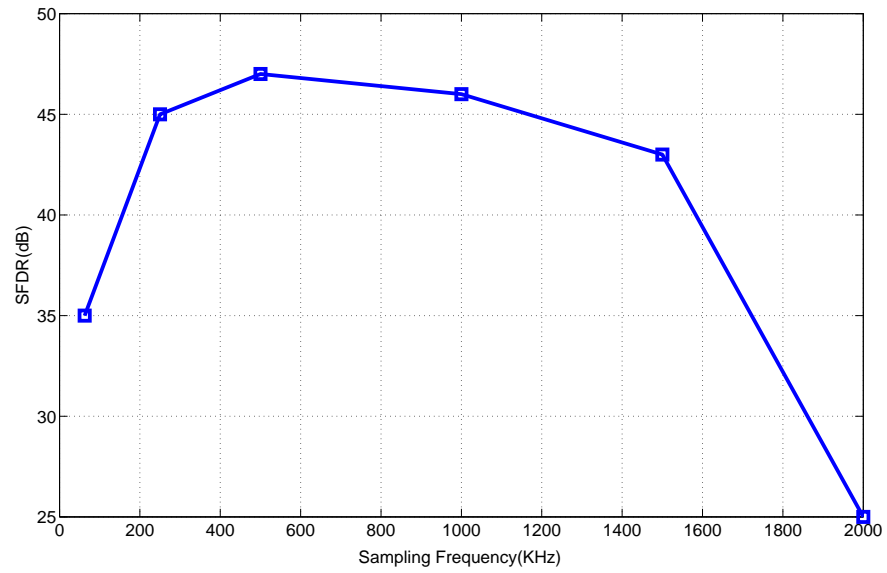


Figure 3.11: Measured Power Dissipation and Spurious Free Dynamic Range Versus Sampling frequency

proves up to sampling rates as low as 62.5KS/s, where degradation starts to occur(See Fig.3.9).

For all values of sampling rate, a linear sampling is guaranteed by the bootstrapped input switches up to frequencies well above Nyquist. For $V_{dd} = .5V$, $F_s = 1.5MS/s$, the resulting converter Effective Resolution Bandwidth is about 2.5MHz. A spurious free dynamic range above 43dB is maintained from $F_s = 250KHz$ to 1.5MS/s(See Fig.3.11). At 2MS/s, the DAC fails to settle to full accuracy, resulting in degraded SFDR of 25dB, and consequently reduced SNDR. At 62.5KS/s the sampling switches leakage is significant, so that SFDR is reduced to 35dB.

Dynamic testing was performed also at supply values different than nominal. As expected, the converter is operational for a wide range of supply voltage and speed values, demonstrating robustness of the design. For $V_{dd} = .75V$ a peak speed of 5MS/s and an ERB of 9MHz are achieved. For $V_{dd} \leq .45V$, the digital logic is subject to critical races that result in sparkle codes and severe SNDR degradation. However, the analog portion of the system(Comparator and sampling switches) is powered through a separate pin and has been measured to be functional for $V_{dd} \geq .3V$ even at a reduced speed of about 300KS/s. A more robust digital logic implementation would have almost certainly guaranteed full system operation at this low-supply, enabling a realistic SNDR testing.

Static linearity was measured through histogram testing; the resulting INL and DNL profile are reported in 3.10. A systematic profile, caused by effects that remain unknown at the time of writing, is apparent.

3.8 Power Dissipation

The measured power dissipation was $14\mu W$, roughly 3 times higher than the simulated value. Table 3.3 reports the individual measured contributions. For different reasons,all of the components show significant deviation from the simulated values.

For digital switching power the discrepancy is due to the fact that parasitics were

not accounted at simulation and design time.

Digital leakage is often poorly modeled. In the specific case, this hypothesis is corroborated by the fact that values as large as 4 times those reported by the model have been measured on other designs fabricated on the same run as this converter. A similar reasoning holds for the comparator, as its voltage-biased pseudo-differential nature makes it intrinsically sensitive to process variations/ threshold voltage modeling inaccuracies.

Although higher than expected, the measured powered dissipation still compares favorably with respect to published works. Also, many circuit techniques are available to reduce the power dissipation of the digital section.

3.9 Comparison with previous work

Many different figures of merits have been defined as metrics to quantify ADC power efficiency. A few definitions are recalled in the following. A very popular metric is the so called energy per conversion step, measured in pJ/conv. This is defined as

$$FOM_{ISCC} = \frac{P_d}{2f_{in}2^{ENOB}}$$

. Here, f_{in} is the maximum signal input frequency for which the effective number of used is used. Ideally, $f_{in} = f_s/2$ and $ENOB = N_b$. The basic assumption here is that doubling the bandwidth doubles the power. Similarly increasing resolution by 1 bit also doubles the power. Although widely used, this figure of merit reflects the scaling behavior of very few practical converters. The most natural application seems to be in Flash converters, which have roughly 2^B comparators; however, increasing the resolution of the converter not only doubles the number of comparators, but puts a twice as stringent offset specification on each comparator as well. This causes the power to scale as 2^{3ENOB} , unless offset calibration is used in the comparators([32]). Even in this case, the assumption of power dissipation being linear in the bandwidth usually does not hold for very high input frequencies, or very low ones. At the high end end of the spectrum, increasing speed in a

circuit that operates in the neighborhood of the devices F_t is known to cost large amounts of power if at all feasible. At the low end of the spectrum instead, leakage gives a background power consumption that is independent of speed.

Another widely used figure of merit is

$$FOM_{Noise} = \frac{P_d}{2F_{in}2^{2ENOB}}$$

. In this case, power is supposed to scale as 2^{2ENOB} , i.e. the cost of increasing the resolution by 1 bit is 4x more power dissipation. This is a fair metric for noise-limited designs, and finds application mostly in high resolution converters, such as $\Sigma - \Delta$ modulators. Looking at the successive approximation architecture, we can observe that

1. Power dissipated by the comparator is linear in the number of bits (adding one bit means adding one extra charge cycling phase) and in the sampling frequency. When noise limitations are taken account, it is furthermore proportional to 2^{2ENOB} , however this constraint is practically active only for high-resolution converters, which are outside the scope of the work.
2. Switching power of the digital back-end is linear in the sampling frequency, and, to good approximation, to the number of bits.
3. Voltage Reference buffer is noise-limited and typically scales as 2^{2ENOB} as well.

In this work, as well as in [25] and in [33], the reference buffer is not implemented, so that the largest contributor to power dissipation that actually does scale as 2^{2ENOB} is not present. In light of these considerations, we introduce a different figure of merit called energy per bit:

$$FOM_{SAR} = \frac{P_d}{F_s B} \quad (3.1)$$

. The main change is that now power is assumed to scale linearly with the number of bits. This is generally true at low resolution, when noise from the comparator is not in issue: for a given sampling rate, going from a resolution of B bits to a

resolution of $B+1$ bits requires all elements in the system to settle in a time interval $B/(B + 1)$ times shorter, i.e. has the same effect of increasing the sampling frequency by $(B + 1)/B$. When the system is digital power dominated, and that leakage is not an issue, this figure of merit still gives a realistic picture of power scaling. In table 3.4, this work is compared to recently published data from similar resolution ADCs using all of three figures of merit. The data indicates one of the best power efficiency ever reported, despite the very low supply voltage.

Design	Resolution	V_{dd}	FOM (pJ/conv.)	FOM_{SAR} (pJ/Bit)	FOM_{Noise}	Tech.
[25]	8	1.4	.24	3.75	1.3e-15	.25 μ
[33]	8	.6	.35	11	2.7e-15	.18 μ
[34]	8	1	26	850	830e-15	1.2 μ
[27]	12	1	.16	15	.12e-15	.18 μ
This work	6	0.5	.2	1.75	4.5e-15	.09 μ

Table 3.4: Comparison with published results

In the figure of merit FOM_{SAR} , this converters outperforms all previously published converters. This is largely dependent on the advanced (90nm) process used, and in part to the aggressive design techniques. A simple calculation shows however the impact of leakage in such an advanced process. The energy per bit of the converter reported in [25] is 3.75pJ/bit. Assuming all of this were digital power, scaling from $V_{dd} = 1V, L = .25\mu$ to $V_{dd} = .5V, L = 90nm$ should automatically guarantee a energy per bit 10 times lower, or .375pJ/Bit. Energy efficiency of the presented design is roughly 4.5 times higher, with leakage contributing a third of the total energy or .6pJ/Bit. This is made clearer by the plot of figure 3.12, which displays the converter Figure of Merit(Energy per Conversion) as a function of sampling frequency.

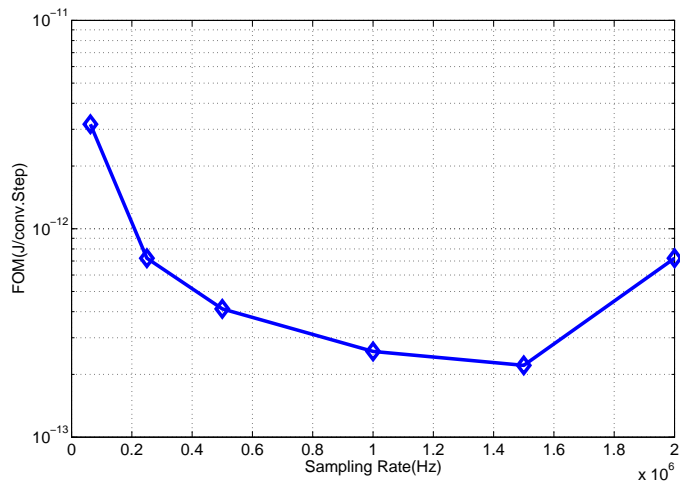


Figure 3.12: ISSCC Figure of Merit as a function of sampling frequency

3.10 Conclusions

This first implementation demonstrated that it is possible to build power efficient converters at a supply voltage as low as .5V . It also confirms our initial analysis showing that unless ad-hoc countermeasures are taken, leakage from the sampling switches results in significant linearity reduction.

Chapter 4

Implementation II: a .5V,6b,1MS/s successive approximation converter with embedded automatic gain control

After the successful design of the first prototype SAR, we decided to pursue integration of the ADC with an RF front-end¹. We describe in this chapter the design of the analog-to-digital converter, and the measured results from its standalone version. Design and measurement results of the RF receiver are described in [35]. The goals of this work were

1. Reduce the power consumption of the digital Back-end, while simultaneously providing a more robust implementation
2. Complete Integration of the ADC sub-system, including voltage reference and driver and clock generation and distribution

¹Designed by N.Pletcher,U.C. Berkeley

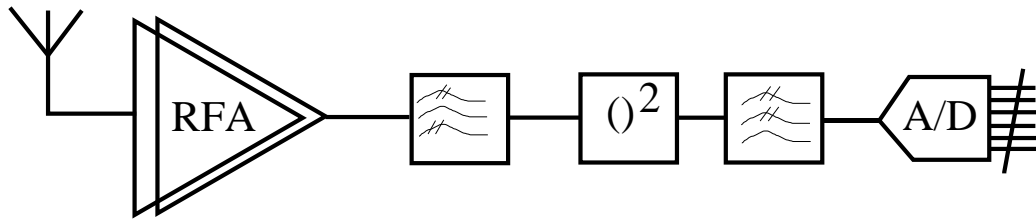


Figure 4.1: Tuned RF radio Architecture

3. Demonstrate the maximum amount of integration reported to date for 0.5V systems with the implementation of the full radio

We further decided to enhance the performance of the A/D converter making use of a digital offset calibration routine, and of a variable output reference, which effectively acts an embedded variable gain function.

4.1 Radio Receiver overview

The combination of front end and ADC is designed to act as a carrier sense receiver for a wireless sensor network radio. System level considerations constrain the total receiver power for this application to about $50\mu W$. Achieving such a power level demands ultimate simplicity in the receiver architecture, which is shown in figure 4.1: a combined of passive/active gain stage precedes the envelope detector, suppressing its noise figure by roughly 20dB and resulting in a sensitivity of -50dBm. A single-stage variable gain amplifier regenerates the signal to the ADC full scale, providing 0 to 42 dB gain and driving the ADC input capacitance.

4.2 Sampling network

We used only standard V_{th} devices in this converter and avoid bootstrapped sampling in combination with high threshold devices, as done in the previous version

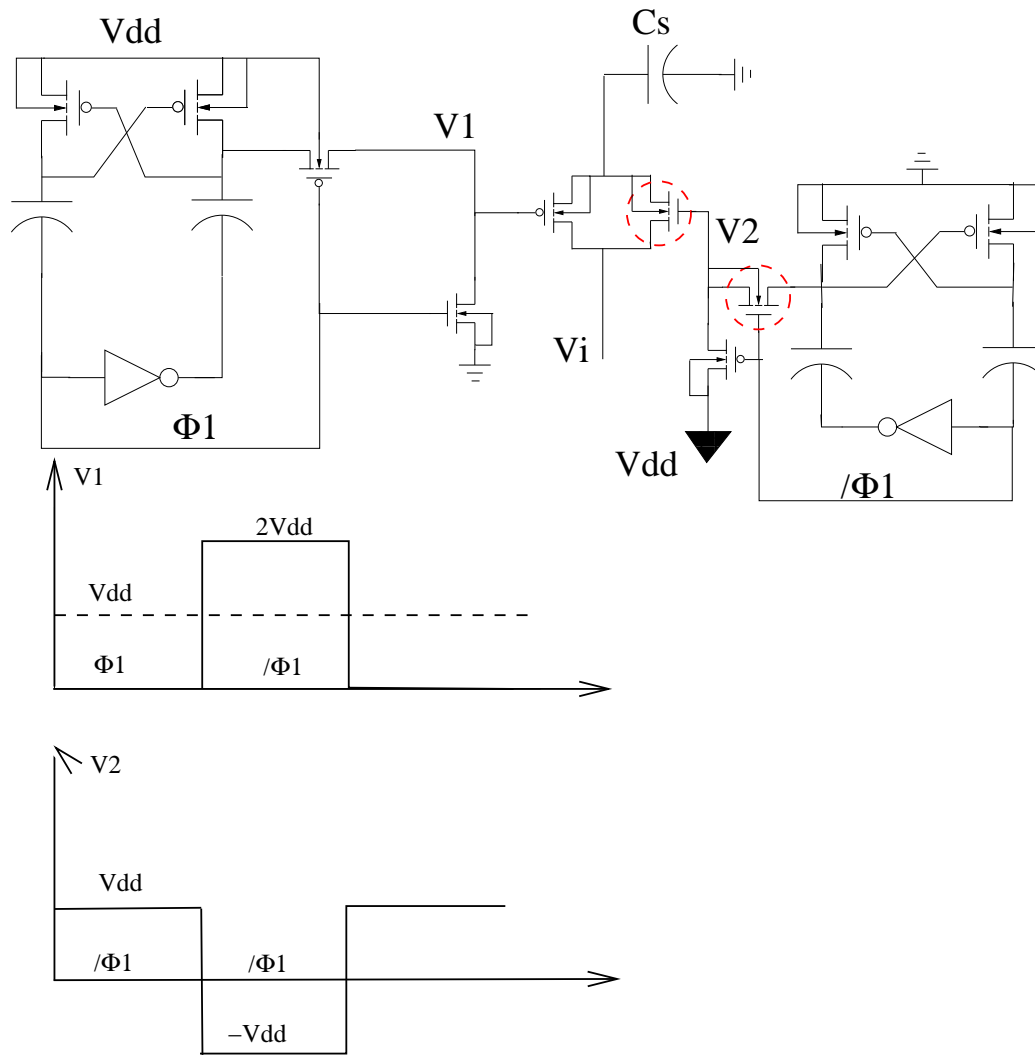


Figure 4.2: Sampling Switch Schematic

of the converter. To avoid charge leakage effects while maintaining sampling linearity, a CMOS switch with complementary boosted turn-off voltage is used. Two separate charge pumps per switch generate voltages of $-V_{dd}$ and $2V_{dd}$, which are respectively used to turn off the n and the p devices. Figure 4.2 reports a simplified schematic. MIM capacitors of 100fF are used as storage devices; the sampling devices have a W/L equal to 10/.1 for the NMOS and to 3/.1 for the PMOS, giving an on-resistance of approximately $30K\Omega$ for each device. Notice that the unusual larger width for the NMOS as opposed to the PMOS is due to the higher threshold voltage of the N device in this process. At low V_{dd} , the resulting decrease in current drive offsets the higher mobility, resulting in lower

conductance per unit width. Finally, note that the devices circled in red in 4.2 are NMOS devices with the bulk tied to the source to avoid forward biasing the drain-bulk junction when the devices passes $-V_{dd}$. This configuration can only be used in a triple well-technology such as the 90nm used in this design. If such an option is not available, the advantages of complementary input switches cannot be combined with of boosted turn-off, with consequent degradation of the dynamic linearity.

4.3 Comparator

The design of the comparator was undertaken with three major goals

1. Increase the input-output isolation, so as to eliminate the series isolation switches and the associated charge injection and timing issues
2. Guarantee high-common mode rejection ratio, so as to minimize the strain on the common mode feedback circuit of the previous stage
3. Maintain an input referred offset lower than 1LSBs in all full scale settings

Goal 1 is easily met by using cascoding on the input transconductor and separating the input and the regeneration branches. Due to the limited headroom, a pseudo-differential input stage is used. This leads to reduced common-mode rejection, and process-dependent bias current and speed. To reduce the sensitivity to process variations, the input stage is digitally programmable with 2-bit precision (not shown in the schematic). To increase the resilience to common mode, a feed-forward cancellation circuit is added. The complete latch schematic is shown in figure 4.3. During tracking mode, devices M9 and M10 act as triode loads to the transconductors M1 and M2. A common mode voltage of 438mV is obtained under typical operating conditions on nodes 1 and 2, corresponding to a small signal gain of -1.4dB; a tracking bandwidth of 10MHz is simultaneously

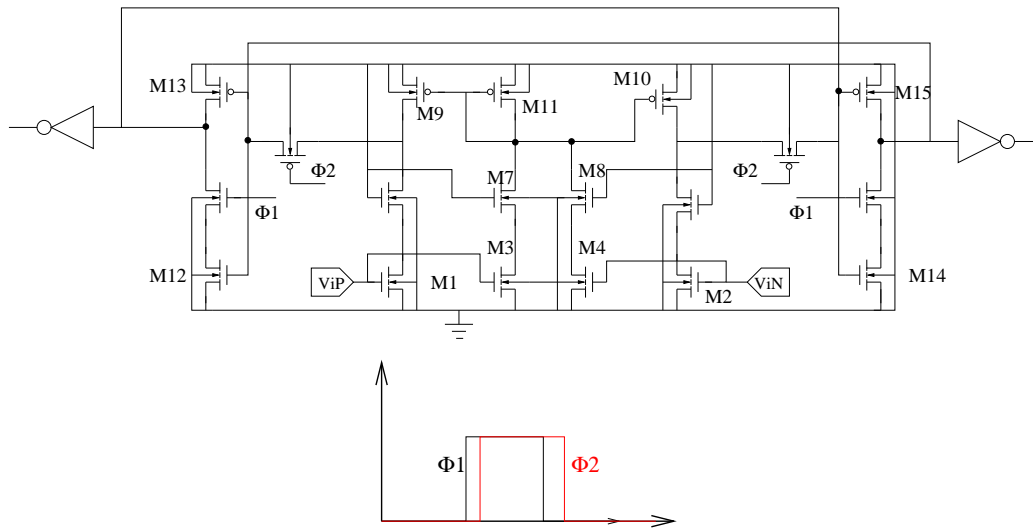


Figure 4.3: Comparator Schematic

achieved. Under these conditions, the common mode cancellation circuit made of M3,M4,M7,M8 and M11 is ineffective due to the low gain through the pmos current mirrors. When a large common mode input step is applied however, the output of the preamplifier is pulled down, activating the common-mode cancellation loop, decreasing the common mode gain and achieving the desired rejection. During regeneration, the transconductor is disconnected from the cross coupled pair with a pair of PMOS switches , and inverters M12-M13 and M14-M15 are enabled and regenerate nodes V_1 and V_2 to the rails, while two more inverter drive the load.

As the LSB can be programmed to be as small as 2mV, an offset variance smaller than $600\mu V$ is required. This offset value can be achieved through sizing at the price of increased capacitance and hence power dissipation. Alternatively, a more complex timing and switching scheme such as the one presented in [27] allows to perform analog offset cancellation. In this project, a different approach is used. Offset cancellation is performed in a mixed-signal fashion introducing an intentional mismatch in the capacitive loading of the regeneration nodes. This approach has been previously proposed([32], [36]); however, it is of particular utility in a SAR converter because, as shown in the following section, it can be implemented in integrated fashion with very small overhead.

It is proved in appendix B that if the capacitive load on node 1 is labeled C and

that on node 2 $C + \Delta C$, an input referred offset of value $V_{io} = \frac{V_{cm}-V^*}{A_v} \frac{\Delta C}{2C}$ is introduced at the input of the comparator. Assuming $C=40\text{fF}$, $V_{cm} = 438\text{mV}$, $V^* = 267\text{mV}$, $A_v = .8$, $\Delta C = \frac{2CV_{io}A_v}{V_{cm}-V^*} = 300\text{aF}$ is found. For the given sizing, on the other hand, a $3 - \sigma$ offset of 24mV was extracted through Monte-Carlo analysis. To calculate the calibration full scale, the more accurate expression(see appendix) $V_{io} = \frac{2(V_{cm}-V^*)}{A_v} \frac{\chi-1}{\chi+1}$ is used. Defined $V^n = \frac{A_v V_{io}}{2(V_{cm}-V^*)}$, $\chi_{max} = \frac{1+V^n}{1-V^n} = 1.1$ and $\Delta C = C(\chi_{max}^2 - 1) = 8\text{fF}$. The required number of levels is therefore $8/.3 \approx 25$ which we rounded off to 31, obtaining a resolution of 5-bits for the magnitude and 1 sign bit for the sign, or a total of 6 bits. Through simulation, a unit element built of $1\mu/.2\mu$ PMOS capacitor and a $.12\mu/.1\mu$ PMOS switch was chosen(See Figure 4.5). Notice that the bulk of the PMOS capacitor M1 is tied to the source to minimize un switched capacitance. In the off state, the whole 31-element array has an off capacitance of 4.5fF , which can be increased in $.8\text{fF/LSB}$ steps.

Figure 4.4 shows a zoomed-in layout capture showing the comparator and the calibration capacitance placed on each side. As any positive-to-negative side imbalance in the routing from the comparator to the capacitance array interferes with the calibration process by introducing offset, care was taken in enforcing layout symmetry. According to extraction, parasitic capacitors of 28fF and 28.5fF are associated respectively with the V_1 and V_2 nodes, showing a mismatch smaller than 1 calibration LSB.

4.3.1 Calibration

We now detail the integration of the calibration logic into the converter. The basic idea is that the calibration routine converts the comparator offset to a digital word, which is applied to a calibration DAC(the switched capacitor array) to cancel it. We perform this conversion process in a successive approximation fashion, so that the calibration capacitors serve as DAC, while the sequencing logic from the converter(see next section) is used to direct the successive guesses.

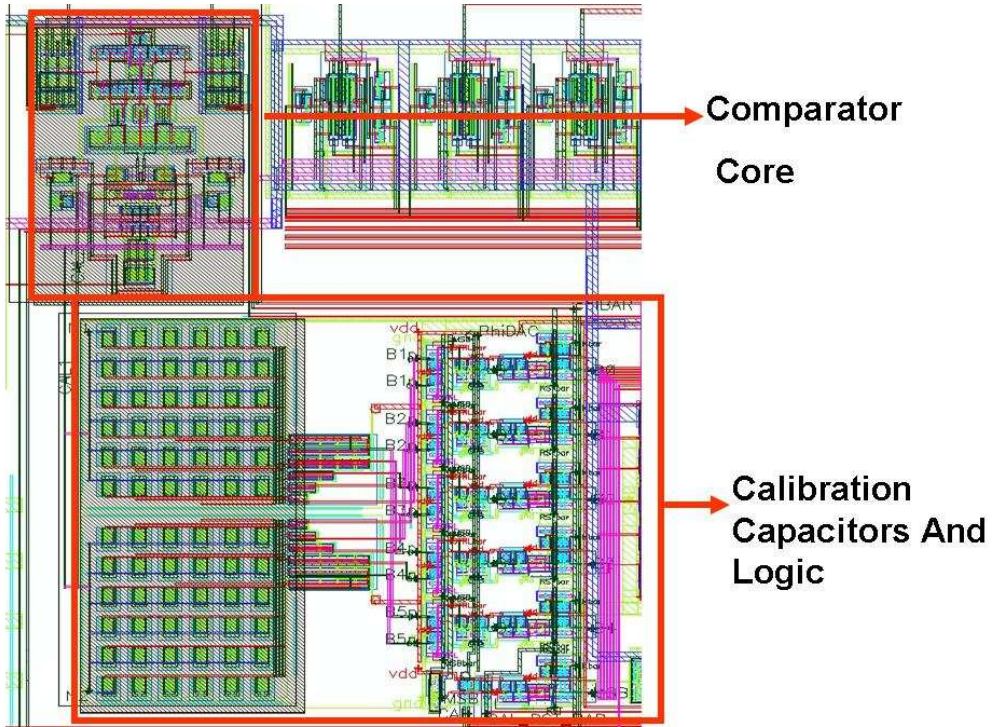


Figure 4.4: Layout of comparator and calibration logic

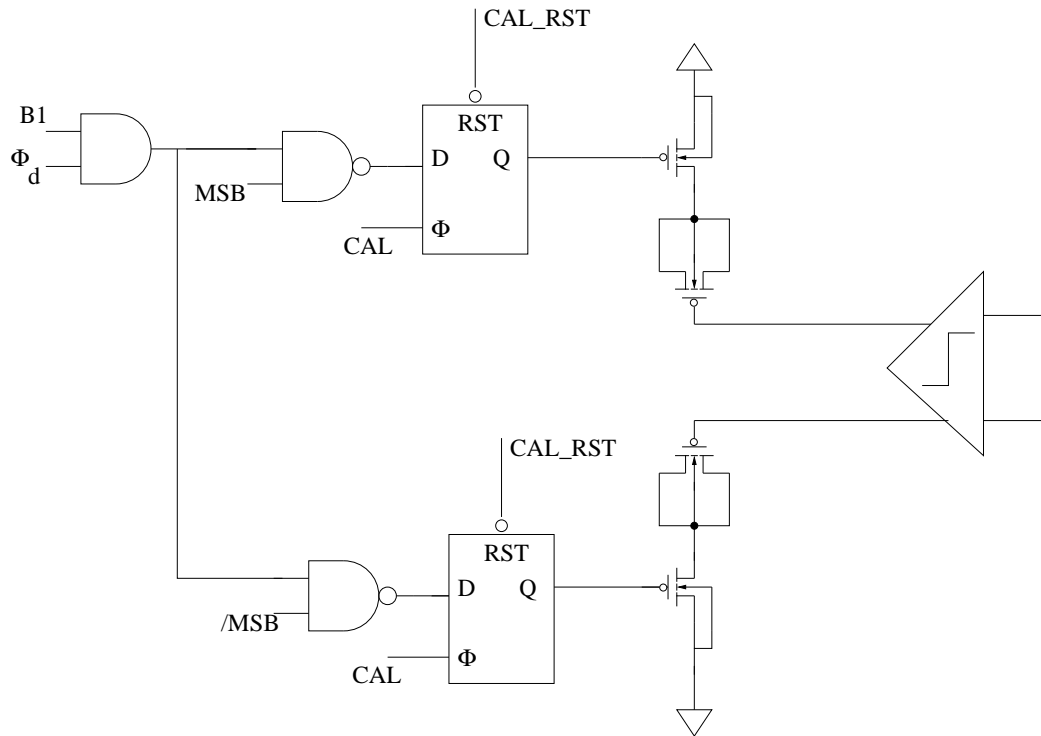


Figure 4.5: Schematic of the calibration logic(only one capacitor is shown)

The calibration routine is as follows: switches $M1$ and $M2$ tie the comparator inputs to V_{cmRef} , while $M3$ and $M4$ are open to disconnect the signal path. The main DAC is disabled by \bar{CAL} . The successive approximation routine is then run for a clock cycle as during normal operation, with the comparator load capacitors acting as DAC. The logic gate G (replicated for each control bit) and the latch F isolate the calibration array from the data conversion array, making their operation mutually exclusive and store calibration code during normal operation. This is shown in figure 4.5.

Notice that the only overhead associated with this technique is in the aforementioned logic and in the extra set of switches. Correct design of these switches is critical to prevent them from perturbing sampling linearity or increasing charge loss. We placed the switches as shown in figure 4.6), *after* the sampling node. This placement minimizes the degradation in sampling linearity; however during normal operation one side of $M1$ and $M2$ is biased at $V_{cmRef} \approx V_{dd}/2$, while the other experiences a time varying potential. This raises the issue of charge leakage

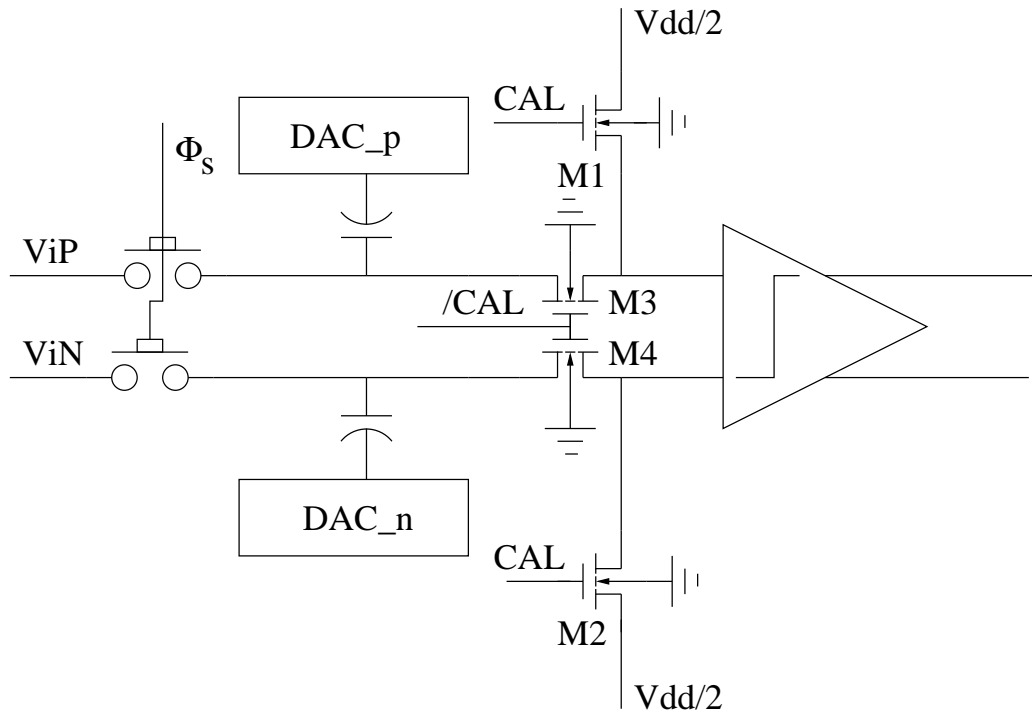


Figure 4.6: Collocation of calibration switches

again. Simulated data show the charge leakage from M2 and M1 during normal operation limits resolution to .25 LSB/s at the maximum full scale, and is strongly reduced by the lower signal swing for other reference settings. In cases where the charge leakage introduced by this switch is not acceptable, but speed is still moderate, the switches could be placed before the sampling switches(4.6), at the price of increased sampling nonlinearity(during normal operation, the aspect ratio of the sampling switch is effectively halved if the switches size is the same.

Notice that as stated before, offsets smaller than 1mV ought to be resolved. If the calibration is therefore run for only 1 cycle, and no code averaging is performed, noise in the converter will limit its accuracy. This limit may be overcome performing multiple calibration cycles in sequence and averaging their result; we claim however that a single cycle calibration will almost surely be sufficient, as even if its resolution is limited by thermal noise, this only means that the ADC residual offset is smaller than the converter noise floor and hence is not going to limit performance.

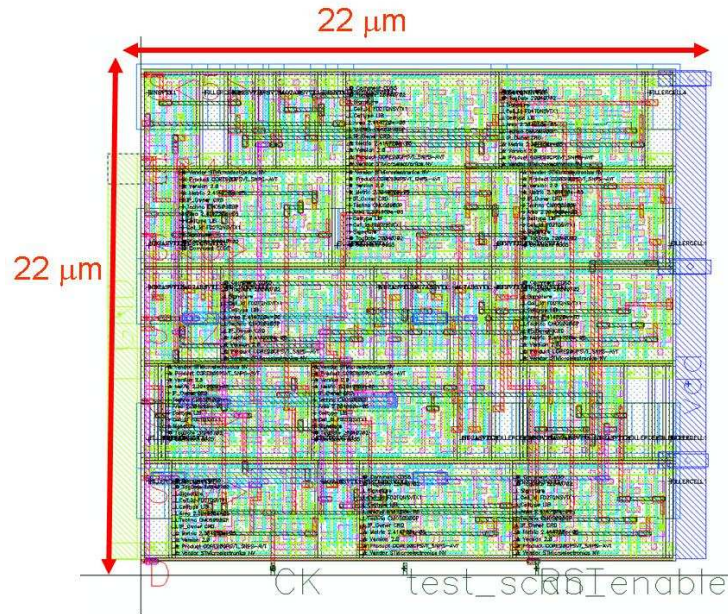


Figure 4.7: Synthesized layout of the digital block

4.4 Digital Logic

The digital logic was implemented by synthesizing a behavioral VHDL description. This approach has the advantage that power minimization taking into account leakage as well dynamic power is performed by the logic synthesis tool under a fixed delay constraint; moreover, the area is reduced compared a not fully optimized hand implementation. To ensure correct operation of the synthesized logic at .5V(the library is only characterized at 1V) we used the approach suggested in [37],consisting in feeding to the synthesizer timing constraints increased by a factor equal to the ratio of the propagation delay of the logic at .5V to the propagation delay of the logic at 1V, roughly 4 for this process. Since the bit cycling period 16 period is $\frac{1}{16MHz}$, a maximum delay constraint of $\frac{1}{4 \cdot 16MHz} = 15.6nS$ is used in this case. The synthesized schematic was imported in cadence and re simulated to verify functionality, which was met over all process corners. Figure 4.7 shows the synthesized layout of the digital portion, which occupies a $20\mu m \times 20\mu m$ area.

4.5 Clock Generator

No self-timing is employed, so that the successive approximation converter requires a fast (bit-cycling) clock as well as a slow (sampling) clock. To minimize power, the sampling clock is bound to have a duty cycle approximately equal to the inverse of the number of cycles. To facilitate testing and for completeness, we integrated the sampling clock generation on chip, using the simple digital logic using a synchronous counter. Only one clock signal is therefore required for correct converter operation. The generated sampling and bit-cycling clocks are fed to a non-overlapping phase generator (See fig. 5.17) that controls the individual blocks. This phase generator occupies an area of $13\mu m \times 28\mu m$ and dissipates less than 200nW at a 16MHz input frequency.

4.6 Band Gap Reference

We have already stated that for low-power designs, reference generation and distribution consumes a significant amount of the power budget. In [25], this bottleneck is avoided by referencing the ADC to V_{dd} . This results in power efficient operation, however, it increases power supply sensitivity, which is typically already poor in low-voltage designs. To show complete integration and true low power design, a fully differential band-gap reference with programmable output was designed. The programmable output feature allows to exploit the quantization noise-limited nature of the companion converter to implement 12dB of variable gain. As explained below, this programmability comes at the cost of increased power dissipation or decreased reference stability.

4.6.1 Core Bandgap design

The band-gap reference concept is proposed in Fig. 4.8. It employs a classical current-scaling architecture, that generates the PTAT and the NTAT voltage in one current branch and combines into a different branch making use of a current mirror. This technique allows to generate sub-1.1V output ([38], [39]), but requires precisely matched resistor to perform the final V-I conversion. Operational amplifier A1 keeps nodes V_1 and V_2 at the same potential, so that the current flowing through the resistor R_1 is $I_1 = \frac{KT \log(8)}{q R_1}$. Since the voltage at node 1 equals $V_1 = \frac{KT}{q} \frac{I_1}{I_{ss}}$, the total current through the current mirror devices reads $I_{ref} = I_1 + \frac{V_1}{R_2} = \frac{KT}{q} \frac{1}{R_2} \left(\frac{I_1}{I_{ss}} + \frac{\log(8)R_2}{R_1} \right)$. If $R_2/R_1 \approx 8$, simple algebra $I_{ref} = \frac{1.12V}{R_2}$; which depends on temperature only through the current defining resistor R_2 . This dependence can be eliminated by forcing this current through a matched resistor of appropriately scaled value, obtaining $V_o = 1.12V \frac{R_3}{R_2}$. This is accomplished by M3 and R3p,R3m. Operational amplifier A2 and current source M4 finally, form a feedback loop that sets the output of the reference to be equal to V_{ref}^{cm} . Compared to other low-power, low-voltage references in [38], [39], this design has a few distinguishing features:

1. At $V_{dd} = 0.5V$, parasitic bipolar transistors cannot be used, as their V_{be} is larger than the supply. Weakly inverted MOSFETs are instead used ([40])
2. The output conductance of the reference should be low enough to drive the DAC input capacitance ($\approx 200 fF$) to 6-b accuracy in 60nS
3. The output should be programmable over 4 levels

Using subthreshold MOSFETs instead of bipolar devices to generate the V_{be} term requires devices Q1 and Q2 to operate in the subthreshold region across the whole temperature range of interest. Assuming the variation in bias current to be small compared to the variations in device specific current I_0 , the worst case is at the minimum operating temperature T_{min} (corresponding to minimum specific current

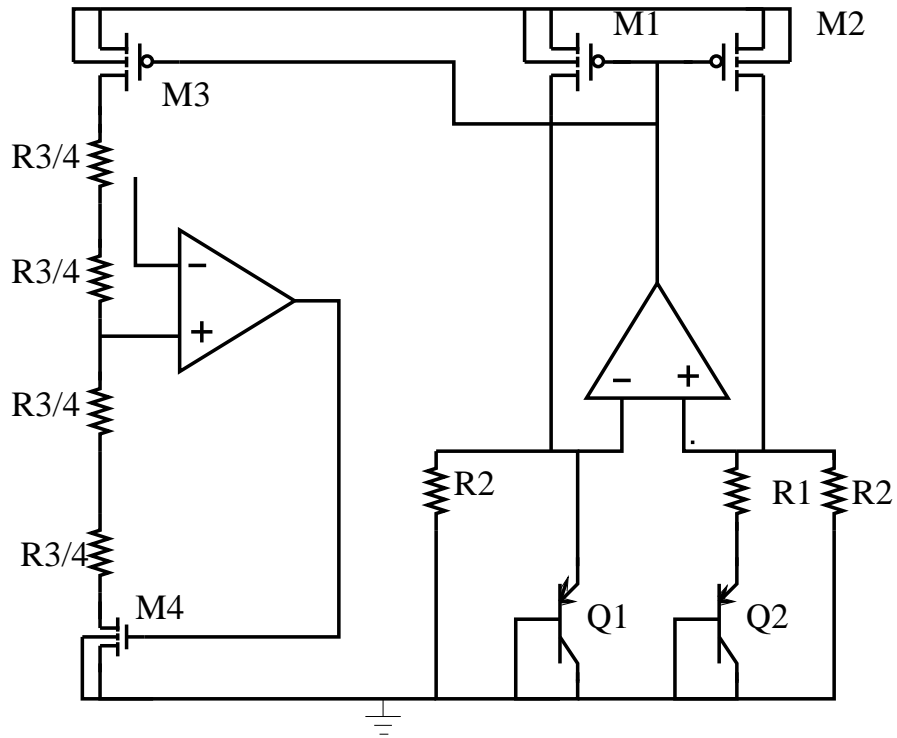


Figure 4.8: Bandgap reference based on resistive division and parasitic bipolar devices

Q1	$9.5\mu/.7\mu$
Q2	$8 \times Q1$
M1,M2,M3	$25\mu/5\mu$
M4	$10\mu/.5\mu$
R_3	$60K\Omega$
R_1	$29.66K\Omega$
R_2	$118.3K\Omega$

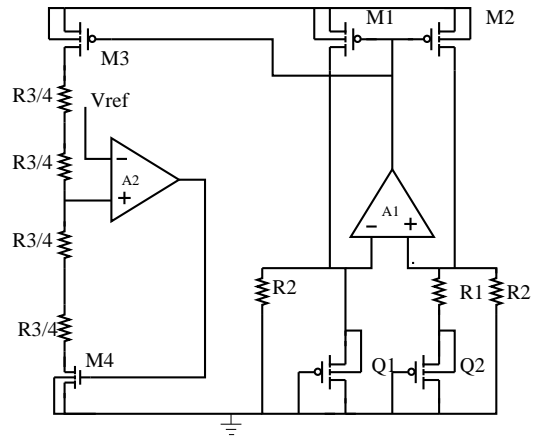


Figure 4.9: Final All MOS Bandgap reference and sizing

value, and hence highest inversion coefficient). This maximum inversion coefficient should be smaller than .3 for the circuit to operate correctly. Assuming these conditions are met, the gate-source voltage of Q2 will be $V_1(T) = V_{th}(T) + \frac{n(T)}{n(T_0)}(V_{gs}(T_0) - V_{th}(T_0))\frac{T}{T_0} \approx V_{th}(T)$ if $V_{gs}(T_0) = V_{th}(T_0)$ [40]. The threshold voltage dependence on temperature is to first order linear, with a slope that depends on device channel length L as $\frac{\partial V_{th}}{\partial T} = K_1 + \frac{K_2}{L}$. Since $K_2 > 0$, device channel length can be tweaked to lower the temperature dependence of threshold voltage, reducing the required value of R_2/R_1 ratio. Following these guidelines, the transistors in this design were sized through simulation to have $W/L = 9.5\mu/.7\mu$. The settling constraint requires an output conductance $R_o \leq \frac{T_s}{C \log(2)} = 72K\Omega$. A power efficient way to achieve this output conductance is to use a diode connected transistor that would give a small signal resistance of $1/gm$; however, this is in contrast with the programmability constraint, as, due to the nonlinear transistor characteristic, building an accurate resistor ladder using diode connected devices is difficult. Linear polysilicon resistors are therefore used. At .5V, the maximum signal output by this architecture is roughly .3V(top and bottom current sources should remain in the active region). From $V = IR$, the current flowing in the output current sources should be $.3V/144K = 2\mu A$. In principle, the current in the reference branch can be scaled to be much smaller than that in the output branch, as it does not influence the settling process. This is however not possible in practice, as too large values of resistance(and hence die area) would be required. The final design choice is influenced by this tradeoff, and the final design values for

the bandgap core are reported in table 4.6.1.

4.6.2 Compensation

Operational Amplifiers A1 and A2 are critical to the correct operation of the circuit: temperature dependent offset from A1 directly adds to the reference PTAT source, degrading bandgap stability; moreover, startup stability of the whole circuit requires stabilization of the feedback loops involving A1 and A2. From behavioral simulations, we found that in order for the circuit to function properly A1 needs a gain of 60dB, while A2 has a more relaxed 40dB gain specification. Therefore, A1 is implemented as a 2-stage amplifier, while a simple differential pair amplifier is sufficient for A2. Both feedback loops are compensated using a Miller strategy. Notice that in the case of A2, a two stage amplifier can be individuated which has A2 as the first stage, and the bottom current source M4 and output resistor R_3 as second stage. As a result, Miller compensation is effective if introduced between the gate of M4 and the common mode sense output. We chose to split the poles and bring the zero back in the left half of the complex plane for robustness reasons. Using a simple RC series block with $R = 60K$ and $C = 5pF$, a phase margin better than 60 degrees is obtained.

The feedback loop involving A1 is easier to stabilize, as the feedback factor is smaller. Being A1 a two-stage amplifier, internal compensation with $C_c = 20pF, R = 60K\Omega$ was sufficient to achieve the desired stability.

4.6.3 Simulated Band-Gap Performance

Our measurement setup did not allow direct performance measurement for the BGR, therefore we report simulation data. As seen in figure 4.11, the output of the final version of the bandgap has in the typical case a positive residual slope that gives rise to a temperature coefficient of 200ppm/C. This residual slope is due to the dummy devices added for matching purposes during layout, and could be

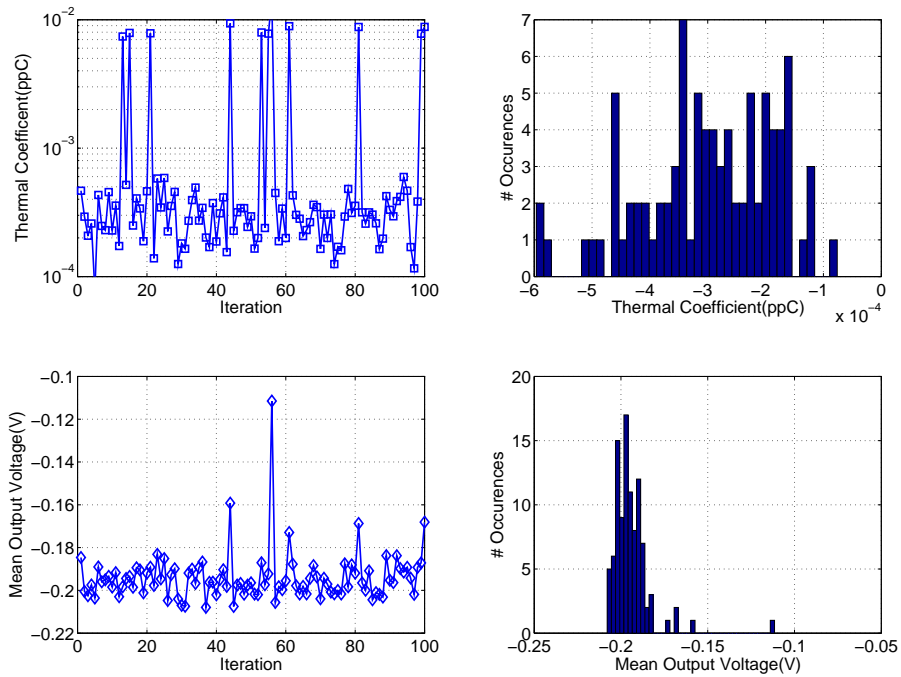


Figure 4.10: Simulated Stability of the band-gap reference

reduced by a proper redesign. Stability over process is also reported in the same context, measured through Monte-Carlo analysis.

4.7 Chip Floorplan and layout

Figure 4.12 shows the top-level view of the converter system. The Band-Gap reference is placed at the top and occupies an area of $120\mu m \times 240\mu m$. Most of the active circuits are placed underneath the compensation capacitors to minimize area. The sampling switch, the digital circuitry and the comparator are placed as far as possible from the reference to minimize coupling through the substrate and capacitive coupling. The sampling switch is further housed in a separate well to maximize substrate integrity.

Two supply pins are used for the whole chip: a core supply is shared between DAC, analog and digital circuits, while a the bandgap reference has an indepen-

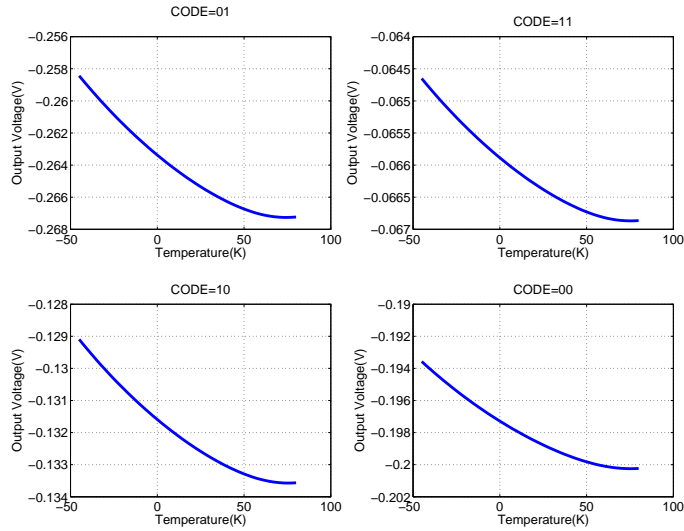


Figure 4.11: Temperature performance in the typical case

dent supply to allow power breakdown measurement. The pins were shorted during on-board during all of the performance testing. To facilitate testing and avoid the timing issues of the previous implementation, the converter outputs are resampled on-chip by the sampling clock.

The total chip active area, including decoupling capacitance, is $350\mu m \times 350\mu m$.

4.8 Experimental Results

The converter was implemented on the same chip as the $\Sigma - \Delta$ converter described in chapter 5 and of the integrated radio receiver described in [35]. Other test circuits are included (See Fig.4.13). The ADC was tested using chip-on-board packaging, with inputs generated in a single ended fashion and converted to differential using an on-board ADI8138 differential driver. The data was read back using a logic-analyzer; MATLAB-based processing as used to quantify performance.

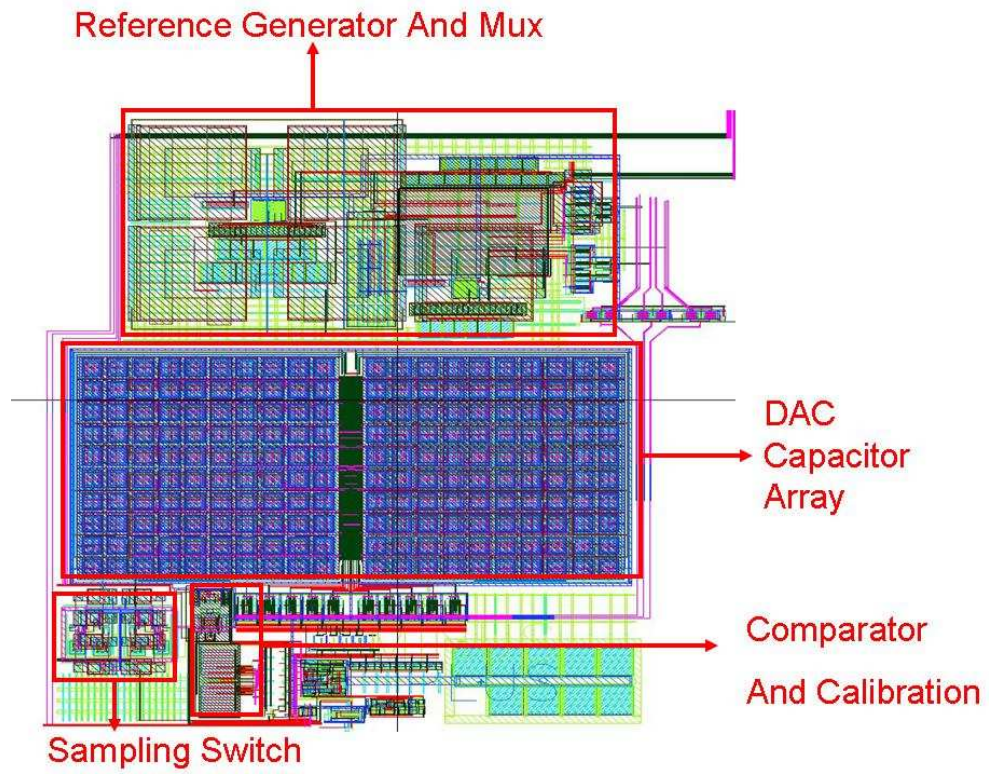


Figure 4.12: Annotated Layout Capture of the Converter Die

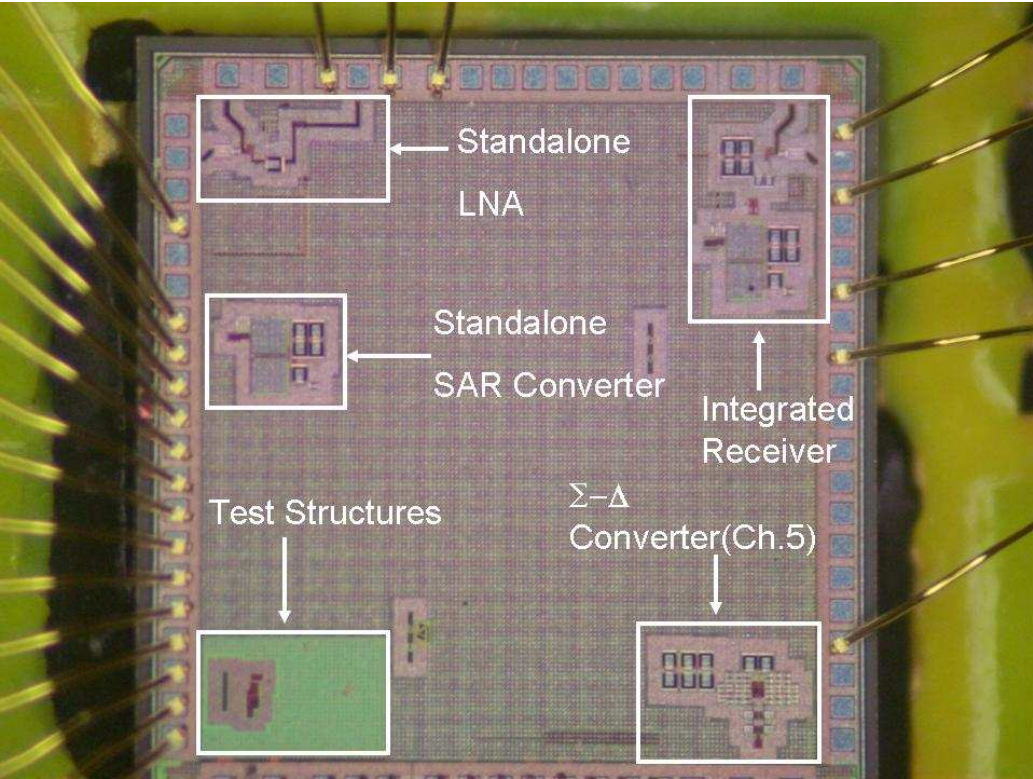


Figure 4.13: Photograph of the complete die

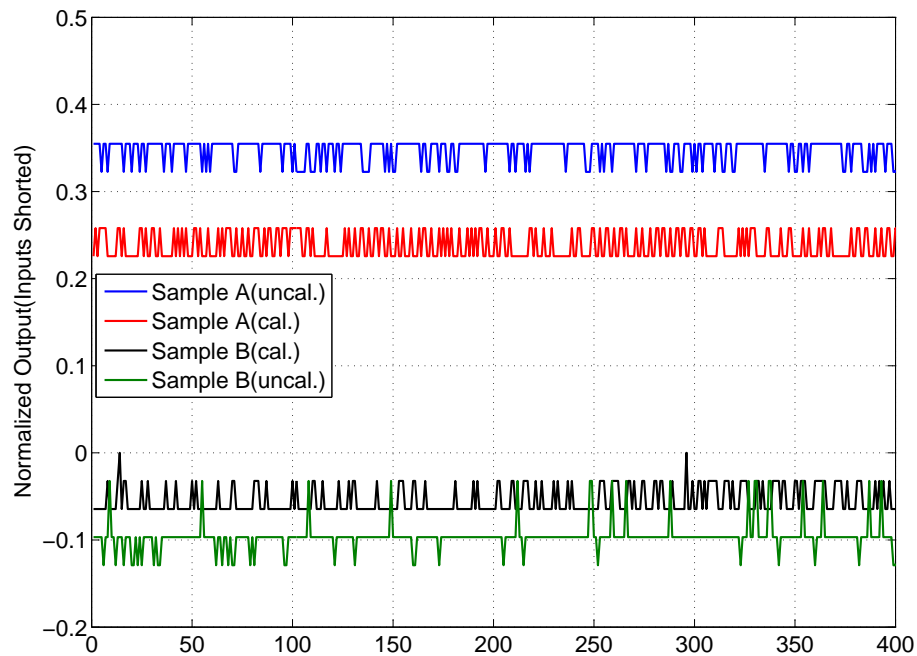


Figure 4.14: Offset calibration results

4.8.1 Offset Calibration

To test functionality of the offset calibration routine, we apply a DC signal such that any DC offset present in the instrumentation is canceled, and the A/D converter input is less than 1mV(measured with a digital multimeter). We then activate the reset calibration signal, which disables all the calibration capacitors ,and measures the converter output referred offset. Then, we raise the calibration signal, and allow the converter to measure its own offset. When the calibration signal is disabled, we measure the output offset again. led, and the A/D converter input is less than 1mV(measured with a digital multimeter). We then activate the reset calibration signal, which disables all the calibration capacitors ,and measures the converter output referred offset. Then, we raise the calibration signal, and allow the converter to measure its own offset. When the calibration signal is disabled, we measure the output offset again. The results of this testing are shown in figure 4.14 for two different samples. Notice that both samples show an input referred

offset which exceeds the predicted value by a large amount. Reasons for this mismatch have not yet been fully understood. This limits also testing of the accuracy of the calibration function, as the measured always exceeds the maximum correction capability. We do see however that the calibration routine always reduces the offset, and that its full scale is roughly equal to 1.5 LSB of the maximum full scale, or 12mV, sufficiently close to the calculated value.

4.8.2 Variable Gain Function

In order to test the embedded variable gain function feature, we feed to the ADC a signal with a swing of approximately 1/4 of the maximum full scale, and then we progressively reduce the full scale of the ADC. In the absence of ADC offset and reference noise, the SNDR should increase by roughly 12dB over the whole range of full scale. The measured data is shown in figure 4.15. As apparent from the figure, the converter residual offset, combined with the reference noise, limit the effectiveness of this approach from the theoretical 12dB to 5.5dB.

4.8.3 Static Linearity

We performed INL/DNL testing by feeding the converter with a 15.111KHz sinewave and collecting 2^{13} samples. Figure 4.16 reports the results. The shape is consistent across full scale settings, and closely resembles the simulated value, dominated by leakage through the calibration switches. However, the negative peak in INL around code 31 was not expected. At the time of writing, the reasons behind this effect have not yet been understood.

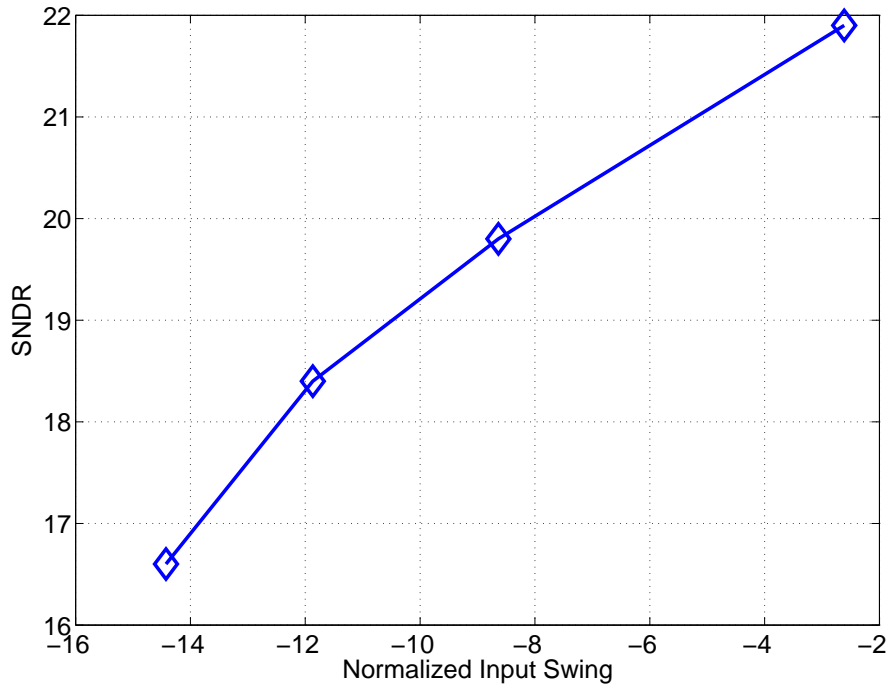


Figure 4.15: Actual performance of the embedded VGA

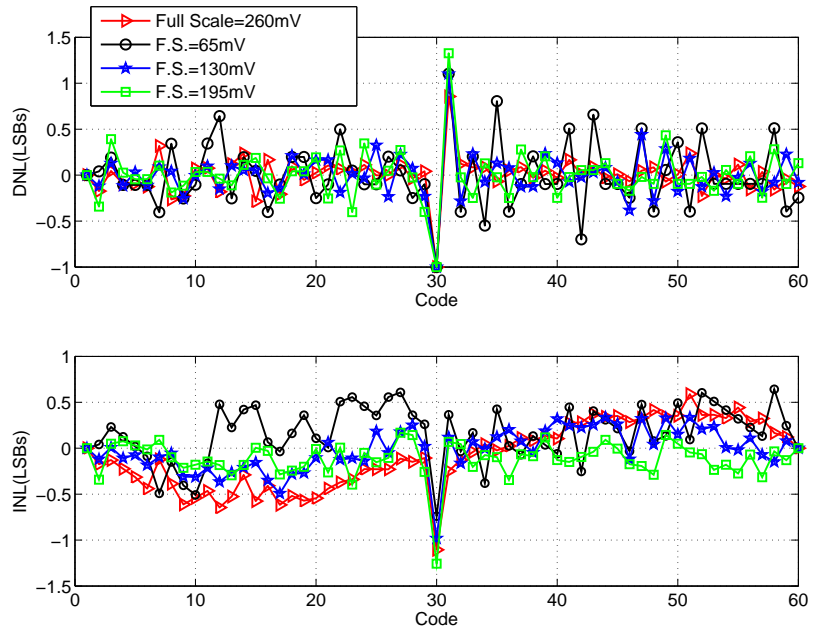


Figure 4.16: Static Linearity for variable full-scale values

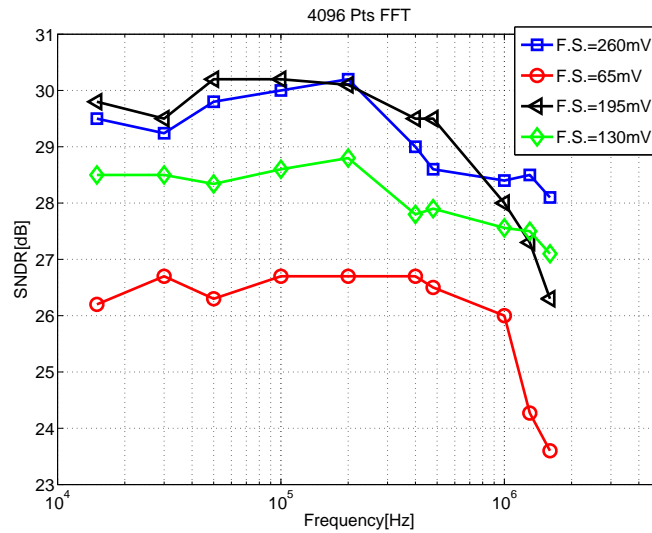


Figure 4.17: Dynamic performance versus input frequency for different full scale values

4.8.4 Dynamic Performance

The performance of the converter for sinusoidal inputs of different frequencies is shown in figure 4.17 for the different full scale settings. A peak SNDR of 30.2dB(4.7 ENOB) is obtained for the largest full scale at 200KHz input frequency. At Nyquist(500KHz), the performance dropped to 28.5dB(4.45ENOB) for the maximum full scale. As the full scale value is decreased, the peak performance shows no degradation for $V_{fs} = 190mV$, while it decreases to 28.8dB for $V_{fs} = 130mV$ ($LSB = 2mV$) and to 26dB for $V_{fs} = 65mV$ ($LSB = 1mV$). This is due to a slightly underestimated band gap reference noise, that becomes comparable with the quantization noise at maximum gain. The performance drops abruptly for inputs above 1MHz, due to limitations in the sampling switch. Figure 4.18 shows the output spectrum for Nyquist rate input of 500KHz. Performance was also measured for different sampling frequencies F_s . In figure 4.19(to the left) the peak SNDR for a rail-to-rail input signal at 15KHz is shown versus sampling frequency. The gradual drop between .75MS/s and 1MS/s is shown in the right half of the plot: the band gap settling is starting to degrade as the

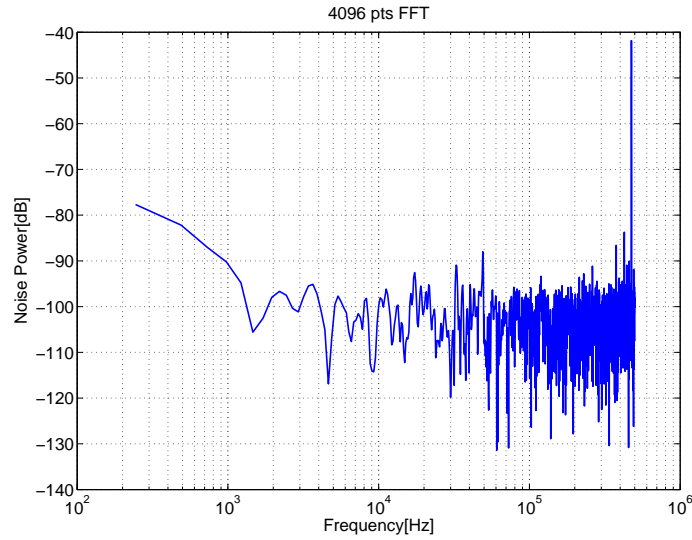


Figure 4.18: Output Spectrum or $f_{in} = 480KHz$

sampling frequency approaches 1MS/s. This reflects in an effective value of $V_{ref}, V_{ref}^{(eff)} = V_{ref}(1 - \exp -T_s/\tau)$ where τ is the time constant of the bandgap settling process. Notice that as band gap presents a very linear output conductance, there is no increase in harmonic distortion as the time available for it to settle is decreased, only swing compression. As expected from the exponential dependence of the effective reference voltage on the sampling frequency however, the degradation is abrupt above 1MS/s.

4.8.5 Robustness to V_{dd}

Low voltage designs, especially if relying on subthreshold operation of devices, has typically been associated with poor robustness. Conversely, the described system operates with power supplies as low as 450mV and as high as 650mV with less than 2dB change in performance, due to the finite power supply rejection ratio of the bandgap reference. This is shown in figure 4.20. The drop in SNDR is related to the finite PSRR of the reference as follows: as the V_{dd} is increased, the reference value increases by $\Delta V_{dd}/PSRR_{lin}$. Therefore, a signal which was

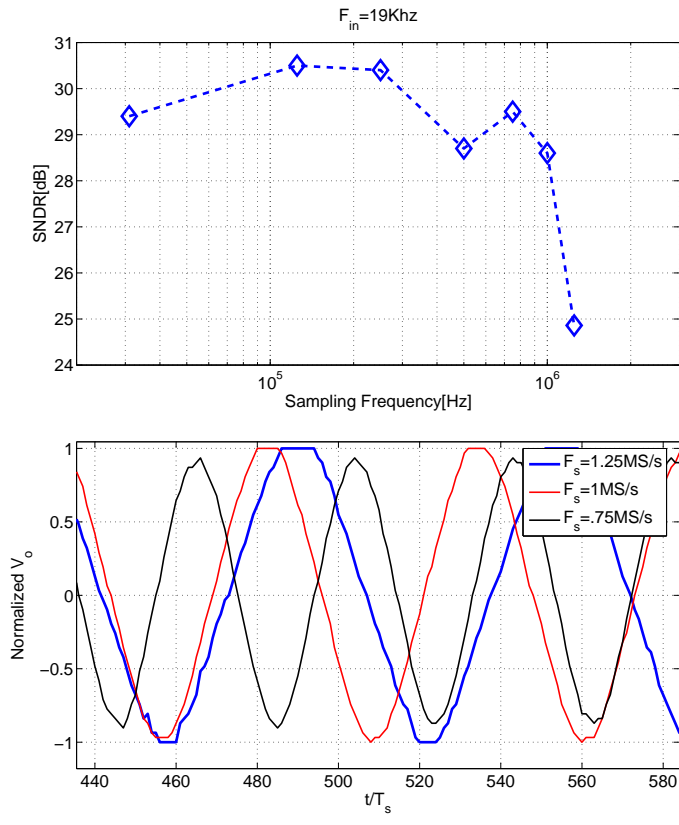


Figure 4.19: Performance of the converter for different sampling frequencies:SNDR(top) and time domain detail of effective referenc reduction(bottom)

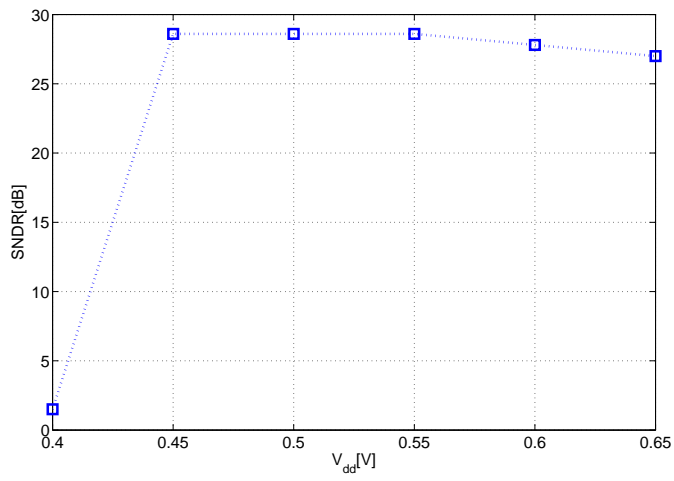


Figure 4.20: Performance variation versus operating supply

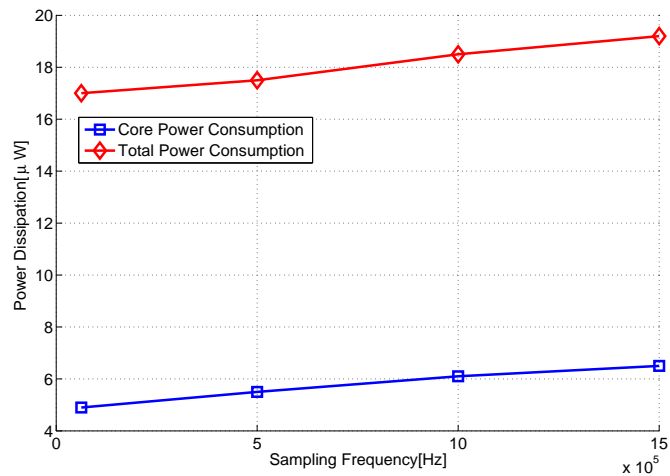


Figure 4.21: Power dissipation versus supply voltage

full scale stops being such, and SNDR drops. The SNDR could be recovered by increasing again the input signal amplitude, so as to match the increased available swing. Notice that the PSRR of the bandgap in this case is only $12dB$ even for DC inputs; the peak PSRR of the reference is about $50dB$, but it is obtained only for $V_{dd} \geq 750mV$, where temperature stability is poor. This is largely due to the fact that PSRR was neglected in the design of the reference; although some effect can be attributed to the compressed signal swing resulting from low supply. It is the author's belief that a PSRR of $40dB$ could be achieved with careful redesign.

4.8.6 Power Dissipation

In the nominal operating point of $1MS/s$, the complete converter system consumes $34\mu A$ from a $0.5V$ supply, corresponding to $17\mu W$. The converter core, comprising comparator, digital successive approximation and calibration logic and clock phase generator, consumes less than $6\mu W$, while about $11\mu W$ are contributed by the reference. The curve of power dissipation versus sampling frequency is shown in 4.22. We can see that the power dissipation is dominated by the variable-output bandgap reference ($11\mu W$) for all sampling frequencies supported. The power dissipation of the converter core is only $6\mu W$ (including analog, digital logic and

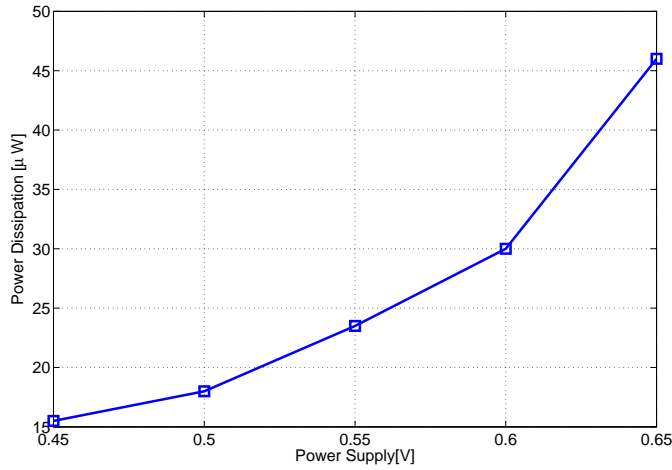


Figure 4.22: Power dissipation versus supply voltage

Block	$P_d(\text{Sim.})$	$P_d(\text{Meas.})$
Reference	$9\mu W$	$10\mu W$
Core	$5.5\mu W$	$6\mu W$

Table 4.1: Simulated and Measured Power dissipation breakdown

clock phases generation and distribution), and again is largely contributed by leakage ($4\mu W$). Again, this contribution could easily be reduced by using high-Vt devices for the digital, if the option is available². Finally, table 4.1 shows the measured and simulated power dissipation values. The matching is very good, and shows the increased robustness of the VHDL-based design flow.

4.8.7 Comparison with literature

This design merges multiple functions into a single low-power building block, making comparison by standard ADC figure of merits challenging. The 6 bits core achieves 4.7 ENOB at 1MS/s for $6\mu W$. If the power efficiency of the converter were quantified by FOM, this corresponds to 230fJ/conversion step, and

²This option was again not available for this design, as low-threshold devices were used in the companion RF-front end

compares favorably to published state-of-the art designs. However, as previously discussed, this figure of merit is not necessarily fair for successive approximation converter cores. Using the previously defined $FOM_{sar} = \frac{P_d}{F_s ENOB}$, we get $FOM_{sar} = 1.25pJ/Bit$, improving over our previous result and competing literature.

Chapter 5

Implementation III: a .65V,100KS/s $\Sigma - \Delta$ modulator

5.1 Motivation and specifications

As we have seen in Chapter 1, in the super-regenerative receiver [10], a significant fraction of power is spent in building a baseband filter for quench tone suppression.

We could trade-off filter performance (and power) for converter performance by simplifying the filter structure, or omitting the filter altogether. If this is done, the converter has to handle simultaneously the quench tone and the signal, and potentially requires a much higher dynamic range. An interesting option is to use a $\Sigma - \Delta$ converter, in combination with no filtering. We claim that an oversampling converter is the optimal solution in this case for two reasons. First, compared with a Nyquist converter where a uniform signal to noise-ratio is guaranteed across the whole $[0, F_s/2]$, a more efficient partitioning of in-band noise and out of band noise is performed, as while oversampling allows to sample out-of-band signals without aliasing, noise shaping ensures that the in-band-noise floor is significantly smaller than the out-of-band noise floor. In other words, since out of band signals

will anyway be rejected, there is no win in wasting power to digitize them to full precision. Second, thanks to oversampling, the pulse width modulated signal at the output of the envelope detector would be directly digitized with negligible aliasing, and demodulation would take place essentially for free as a by-product of decimation in the digital domain. This gives a significant programmability advantage over an analog implementation, and, depending on the cost of the decimator in terms of power, can also give a power advantage. Furthermore, it enables the use of a lower quench-frequency to data-rate ratio, opening the potential to achieve higher data-rates in a super-regenerative receiver. In order for this approach to be appealing the power spent to perform oversampled A/D conversion, including decimation, should be smaller than the power necessary for baseband filtering and subsequent Nyquist A/D conversion. Given that the baseband filter in [7] consumes $32\mu W$, and that we have shown that Nyquist A/D conversion can be performed at the performance level required by the application for only a few microwatts, the power dissipation of the modulator and the the decimator should be below $32\mu W$. Recently, Yao ([26]) has shown that the cost of a 14-bit precision 40KS/s decimator integrated in 90nm standard digital CMOS is of the order of $10\mu W$. Therefore, a power budget of $20\mu W$ is allocated to the modulator. The power supply is chosen to be .65V to ensure compatibility with future process technology and simplify the low-power decimator design.

The super-regenerative receiver of [10], supports a maximum data-rate of 20Kbs, limited by quench-suppression filter. Considering the potential decrease in quench tone to symbol frequency ratio, we designed for a 100KS/s nominal converter speed. Finally, we set the design goal for dynamic range to 70dB.

These specifications correspond to a challenging figure of merit (FOM) of .12pJ/Conversion step, lower than any published Nyquist rate or oversampling converter. Achieving such an extreme power efficiency requires careful design at the architecture and at the circuit level.

5.2 High level modulator implementation choices

The variety of solutions available in the design of an oversampling converter makes systematic exploration prohibitive. We focus on a few assumptions that influenced the results achieved in this work.

1. Recently, Continuous Time $\Sigma - \Delta$ (CTSD) modulators have emerged as the preferred solution to implement highly power efficient converter with bandwidths in the MHz range [41]. A continuous-time loop filter presents a built-in anti-alias filtering function and typically requires lower bandwidth in the operational amplifiers with respect to the sampled-data counterpart. Although the application of CTSD to lower bandwidth scenarios is appealing, it presents an issue: in CT modulators, the converter noise floor is usually dominated by the input resistors of the first integrator (assumed to be implemented in active RC fashion). For moderate resolutions and small bandwidth, this results in very large input resistors, which are hard to integrate on-chip unless high-resistance polysilicon is available [16]. This means that in our scenario, the resistor size would be limited by size constraints, and operational amplifier noise would most likely dominate the converter floor. Therefore, a non-standard design methodology should be devised and used. At the time this project started, this issue was only one of the many of the many unknowns on the strategy to follow to minimize power dissipation in a CT modulator. We therefore chose to implement the converter using a switched capacitor loop filter, for which the literature corpus is much larger and the design methodology more established.
2. Feedforward loop filter realization has also gained increased popularity in recent years. In particular, the authors in [42] show that a spurious free dynamic range in excess of 100dB is achieved with only 60dB gain in the operational amplifiers by introducing feedforward coefficients in the loop filter in order to suppress the portion of input signal manipulated by the first integrator. Although this technique is very appealing in the context

of data-acquisition, its applicability to communications is hampered by the degraded robustness to out-of-band interferers that typically accompanies feedforward loop filter implementations. As one of our goals is to minimize the amount of filtering to be performed upfront the modulator, we decided to use a more robust feedback loop filter. As a result, linearity is only determined by the open loop-gain of the first operational amplifier, and can be harder to achieve.

5.3 Project philosophy

The goal of this work was to minimize power dissipation of a $\Sigma - \Delta$ modulator, given performance constraints. Our approach to this problem was to assume that minimum power consumption is achieved by relaxing as much as possible the key building specifications, with the idea that *finding the least restrictive set of constraints of critical parameter values that would produce in the required performance, would yield the most elegant and most power efficient solution.*

The key block in every $\Sigma - \Delta$ modulator implementation is the first integrator, which determines noise and distortion performance of the whole converter. Although passive integrator implementations have been proposed ([11], [43]) they usually require fairly large capacitor ratios to realize the desired transfer function; while the lack of input output isolation makes the loop filter design challenging. We therefore decided to use an operational-amplifier based integrator. As a result, the operational amplifier becomes the main focus of our power-minimization effort. Results from the analysis reported in chapter 3, as well as results stated in a following section, indicate that a single stage operational amplifier is an optimal choice for low-power designs. This assumption of optimality of a single stage amplifier in an environment where cascoding is not available due to the low supply and flicker noise is a significant concern due to the low-frequency operation drove all the assumptions made in the next section. In particular, a hard cap of 40dB was imposed on the open loop amplifier gain to ensure single-stage realizability.

5.4 MATLAB modeling environment

5.4.1 Motivation

In a previous chapter, we identified gain as the specification hardest to achieve in low-voltage environments. In order to minimize power, our effort was devoted to evaluate the minimum operational gain necessary to achieve a given linearity, and use that as a design target. The topic of integrator nonlinearity is addressed in [44] using Taylor series expansion. However, the analysis is targeted at evaluating nonlinearities introduced by the sampling and integrating capacitors rather than by the integrator nonlinear gain itself. The topic of integrator integrator gain effect is treated both in [44] and in [45], [26]. However, the former work targets a very high dynamic range of 100dB; while the latter ones limit themselves to evaluating the effect of integrator linear gain on quantization noise suppression. When the latter type of analysis is performed, typical integrator gain values in the range of 25dB to 30dB are found for three stage modulators. Designs in [45] and [26] report that their operational amplifier gain was overdesigned from this value in order to suppress distortion. The net result is that the relationship between amplifier open loop gain and nonlinear distortion is not accurately quantified nor well documented. In order to fill this information gap, a behavioral model that takes into account integrator gain value and shape accurately while ensuring simulation time significantly shorter than the full device level simulator is required.

5.4.2 Object Oriented Modulator Model

For execution speed reasons, we preferred MATLAB to simulink modeling. Also, the command line based interface in MATLAB guarantees higher abstraction, and helps carrying on the design in a structured fashion rather than by tweaking individual block parameters. We increase the effectiveness of using MATLAB by using an object oriented approach, similar to the philosophy of class programming

in e.g. C++: a modulator is seen as an object built of different components, each of which belongs to a separate data type. The modulator can be modified by using member functions, that make sure that the underlying modulator components are handled in a consistent way. We postulate that an N_{th} -order modulator is uniquely specified by the following fields:

1. A N-dimensional vector of integrator sampling capacitors, labeled C_s
2. An N-dimensional vector of integrator load capacitors (meaning capacitance connected between the integrator output node and ground), labeled C_L
3. An N-dimensional vector of integrator closed loop gain G_{cl}
4. An OTA object. Note that in principle, N OTA objects should be used. However, because the non-idealities are always dominated by the first integrators, the remaining N-1 amplifiers are assumed to behave ideally.
5. A scalar parameter F_s , equal to the modulator sampling frequency
6. A scalar parameter V_{ref} equal to the feedback reference voltage

The core step of the modeling is the integration step, which is tightly coupled with the OTA object model. Both are described in the following subsection.

5.4.3 Integration Step

We start with considerations on the settling of a switched capacitor integrator with finite operational amplifier gain, bandwidth and slew rate and then extend to the case of nonlinear gain. For the circuit of figure 5.1, neglecting for now amplifier bandwidth and slew-rate and assuming the initial voltage at the integrator output is $V_o(k)$, and the input is V_i , the voltage at the output at time step $k+1$ is

$$V_o(k+1) = V_i \frac{G_{cl}}{1 + \frac{G_{cl}}{A_v}} + V_o(k) \left(1 - \frac{\frac{G_{cl}}{A_v}}{1 + \frac{G_{cl}}{A_v}} \right) \quad (5.1)$$

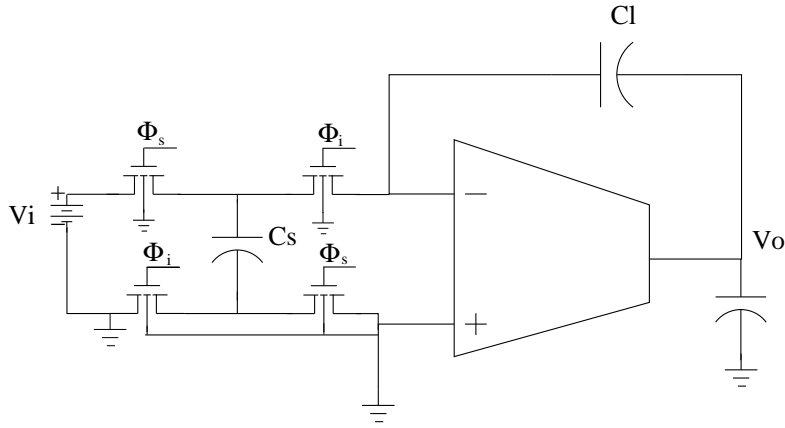


Figure 5.1: Switched capacitor integrator model

, where $G_{cl} = \frac{C_s}{C_i}$ is the ideal closed loop gain, and A_v is the amplifier open loop gain. This is however only the ideal final value of the OTA output in case infinite time were allowed for it to settle. In order to get a more accurate relationship, we need to include slewing and finite settling speed in the analysis. By making a dominant pole approximation for the amplifier response and neglecting slewing, we find that the amplifier response obeys the equation:

$$V_o(t) = V_o(KT) + V_i G_{cl} \left(-\frac{s_p}{s_z} + \left(1 + \frac{s_p}{s_z}\right) (1 - \exp -t \cdot s_p) \right) \quad (5.2)$$

$$s_z = \frac{G_m}{C_I} \quad (5.3)$$

$$s_p = \frac{F G_m}{C_L + \frac{(C_s + C_p)}{1 + G_{cl}}} \quad (5.4)$$

$$F = \frac{C_s}{(C_p + C_s) G_{cl} + C_s} t \in [0, T_s] \quad (5.5)$$

The response of a real amplifier deviates from the equation above due to the amplifier finite output driving capability, giving rise to the phenomenon

$$t^* = -\frac{1}{s_p} + \frac{|V_i| G_{cl} \left(1 + \frac{s_p}{s_z}\right)}{SR} \quad (5.6)$$

$$T_{slew} = \max(t^*, 0) \quad (5.7)$$

$$V_o(t) = V_o(KT) - V_i \frac{s_p}{s_z} + \text{sign}(V_i) \cdot SR \cdot t \quad t \in [0, T_{slew}] \quad (5.8)$$

$$V_o(t) = V_o(T_{slew}) + \left(V_i G_{cl} \left(1 + \frac{s_p}{s_z}\right) - \text{sign}(V_i) \cdot SR \cdot T_{slew} \right) \cdot \left((1 - \exp -(t - T_{slew}) \cdot s_p) \right) t \in [T_{slew}, T_s] \quad (5.9)$$

Substituting the expression for t^* into 5.9 and taking derivatives, one can obtain analytical estimates of slewing nonlinearity as a function of other design parameters. The next effect to be added in the model is integrator nonlinear gain. In this application, the most important features of the model are the possibility to trade increased accuracy for increased simulation time at design time in an intuitive way. The number of parameters in the model is not important and can be large. For these reasons we chose to implement a piecewise-linear gain mode which has the advantage of being very intuitive and to provide potentially very high accuracy. The shape of the amplifier gain versus input voltage is approximated by a staircase function. For simplicity, we assume this staircase to be symmetric, so that we need to store its values only for positive inputs. Now consider the problem of computing the integrator output voltage, given input voltage V_i and initial condition $V_o(k)$. As in the linear case $V_o = V_o(k+1) = V_i \frac{G_{cl}}{1 + \frac{G_{cl}}{A_v}} + V_o(k) \left(1 - \frac{\frac{G_{cl}}{A_v}}{1 + \frac{G_{cl}}{A_v}}\right)$; $V_x = \frac{V_o}{A_v}$ must hold simultaneously, but now A_v is a function of V_o . We can solve this equation by iterating over these two steps: given a gain estimate $A_v(n)$, compute $V_o(n)$ using equation 5.1. Compare now $Av(V_o)$ and Av_n : if they are different update $A_v(n+1) = Av(V_o)$ and repeat, otherwise stop. For realistic parameters values ($A_v \geq 10$), this iteration always converges; furthermore as a consequence of the staircase approximation, we are guaranteed that this convergence will be achieved in a finite number of steps. Of course, the finer the staircase approximation, the longer the convergence, the better the accuracy. This completes the algorithmic part of the integrator model; while the question of how to obtain the parameters necessary to run the model itself is still to be answered. This is very much dependent on the application of the model. In an early design stage, when a $\pm 30\%$ accuracy w.r.t. transistor level simulation is adequate, using calculated parameters is preferable. If however the model is used to speed-up the verification of an almost complete design, then simulated values should be used, especially for the large signal amplifier gain. Extracting amplifier slew-rate and unity-gain bandwidth requires only a transient and an ac analysis, while extraction the large signal can be performed using a dc sweep. The computational cost of these analyses is negligible, while their results guarantee to extend the accuracy of the model to a few percents.

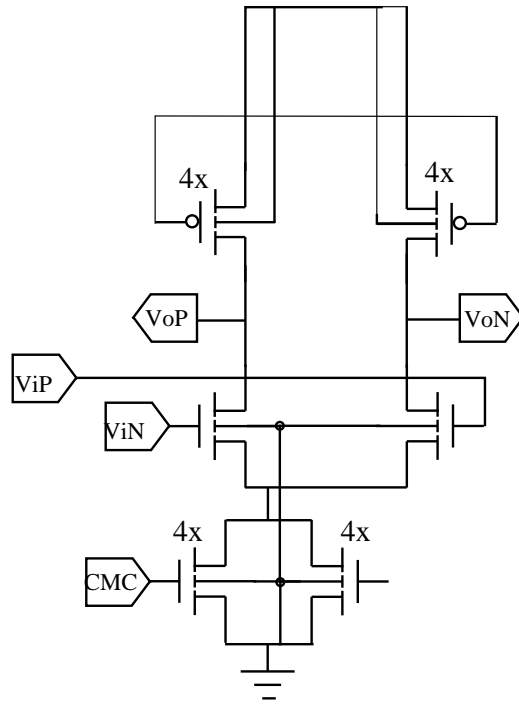


Figure 5.2: Differential pair OTA used in model validation

5.4.4 Model Validation

To validate the integrator model, we tested its accuracy against a transistor level simulation of a conventional bottom plate sampling integrator, where the sampling switches were replaced by ideal AHDL switches, while the operational transconductance amplifier was a simple differential pair amplifier shown in figure 5.2. We used an 8 bin-piecewise linear integrator model for this comparison. The results are shown in figure 5.3,5.4. And show excellent agreement. Since we neglected secondary effects such as switches leakage and charge injection using ideal switches and as the OTA used for this comparison has a true single pole response, these results are probably optimistic with respect to how well the model would do in a general case(more complex simulation setup/amplifier).

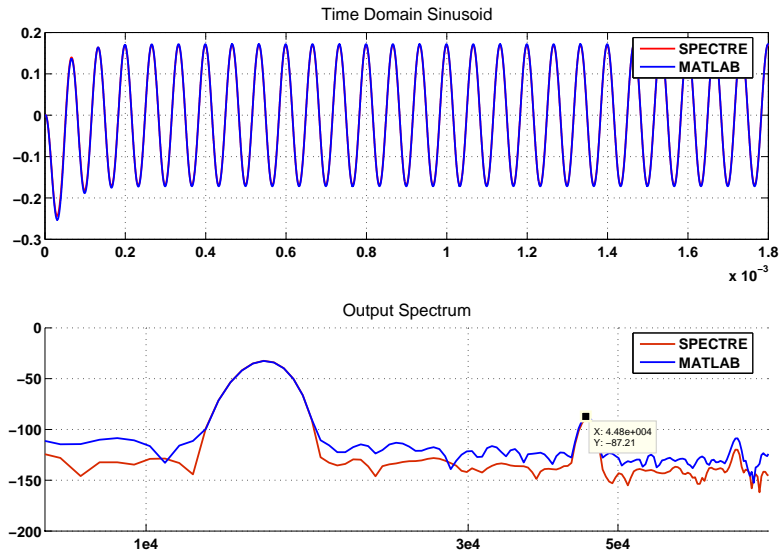


Figure 5.3: Model accuracy for sinusoidal input. Full scale is .3V zero-peak. Predicted third order nonlinearity is within 1.5dB of simulated one

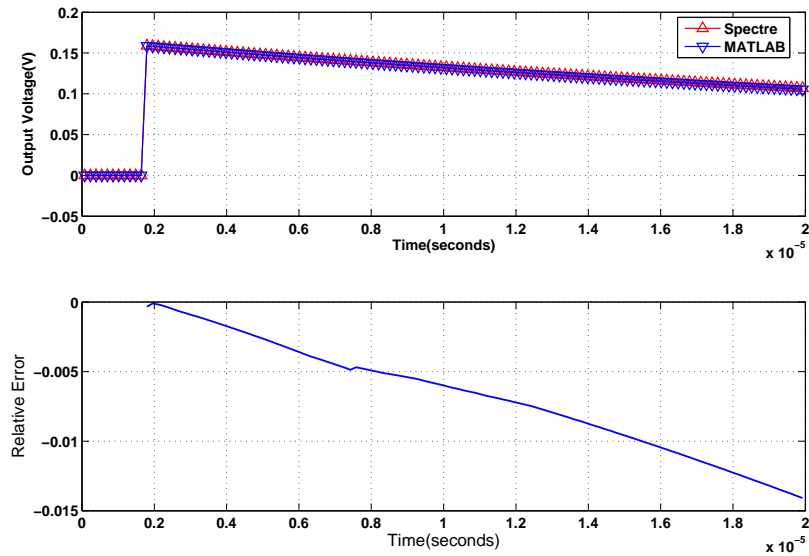


Figure 5.4: Model accuracy for integrator impulse response

5.4.5 Modulator Model

We build on this routine to construct a complete modulator model. Two different versions of the model have been implemented, one supporting half delaying integration, and the other one not supporting it. The first version differs from the second in that a conditional loop that keeps track of the different clock phases and accordingly updates only the outputs the integrators which are enabled in that phase; this enables accurate modeling of e.g. switched op-amp modulators, where the integrators are intrinsically half delaying. The presence of this conditional loop, however, seriously degrades execution speed.

5.5 Loop Filter Design

We focused our attention on second and third order, feedback based loops, as higher order loops tend to compromise stability or reduce signal swing. For infinite integrator gain, the Signal-to-Quantization-Noise-Ratio(SQNR) of a K-th order modulator is written as

$$SQNR = 6\alpha^2 \frac{OSR^{(2K+1)}(2K+1)}{\pi^{(2K+1)}} \quad (5.10)$$

Here OSR is the oversampling ratio $OSR = \frac{F_s}{f_N}$, while α is the input signal measured with respect to full scale. Usually, the SQNR should be 6 to 10dB higher than the final SNDR to be obtained, and should therefore be about 80dB for $\alpha = 1$. Furthermore, while formula 5.10 assumes an NTF of $(1 - \frac{1}{z})^K$ and ideal integrators, real loop filter response and finite integrator gain result in deviations from the value in 5.10. Assuming the conditions stated above hold, and assuming $\alpha = 1$, a second order modulator needs an oversampling $OSR = (\frac{SQNR \cdot \pi^{2K+1}}{6})^{\frac{1}{2K+1}} = 64$ to achieve a SQNR of 80dB, while a third order modulator only requires $OSR = 26$. A second order modulator seems therefore adequate to meet our specifications. Furthermore, values of α approaching unity are harder to achieve for higher order modulators. The loop filter coefficients have been chosen exploring through simulation different configurations starting from

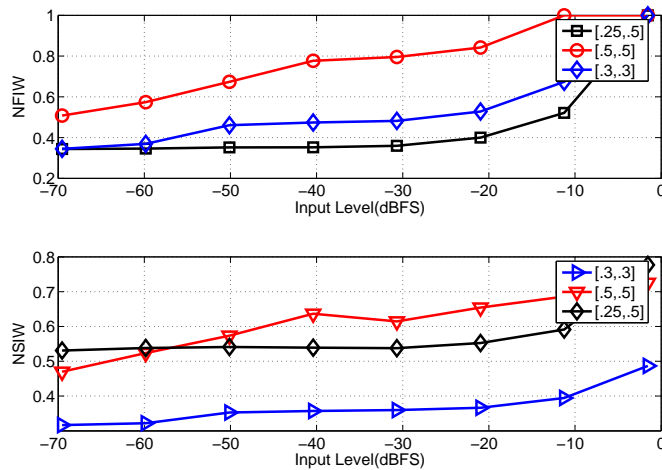


Figure 5.5: Normalized integrator swings for the (.3,.3), the (.25,.5) and (.5,.5) configurations

the (0.5,0.5) value reported in [44]. Amplifiers with finite gain of 40dB but otherwise ideal were used for this purpose, while the oversampling ratio was set to 128. As shown in figure 5.5, the configuration (.3,.3) behaves better than the (.5,.5) with respect to integrator swings, while it provides similar SQNR for a given oversampling ratio. Figure 5.6 reports the simulated output spectrum for input signal of $-70dBFS$. Limit cycles being present in the converter unless amplifiers with open loop gain higher than 46dB are used.

To overcome this problem, one could either increase the amplifier open-loop gain, increase the modulator order or use a MASH architecture. The latter choice was discarded because of the high sensitivity of the recombination filter to amplifier finite gain. Although this limitation could be overcome by using digital calibration of the recombination filter coefficients at power up ([41]), we decided not pursue this road. We further claim that increasing amplifier open loop gain beyond 40dB has a significant cost in power dissipation, as because of cascoding not being practical at a low supply, a two stage topology should be used. On the other hand, because of noise scaling, increasing modulator order, if precautions are taken to preserve signal swings, comes at a minimal price in terms of power dissipation. Figure 5.7 shows the simulated output spectrum of a third

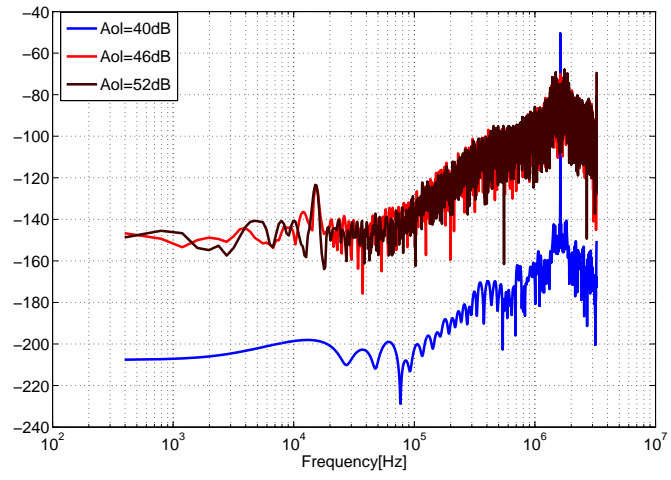


Figure 5.6: Output Spectrum for $-70dBFS$ Input Signal for second order converters

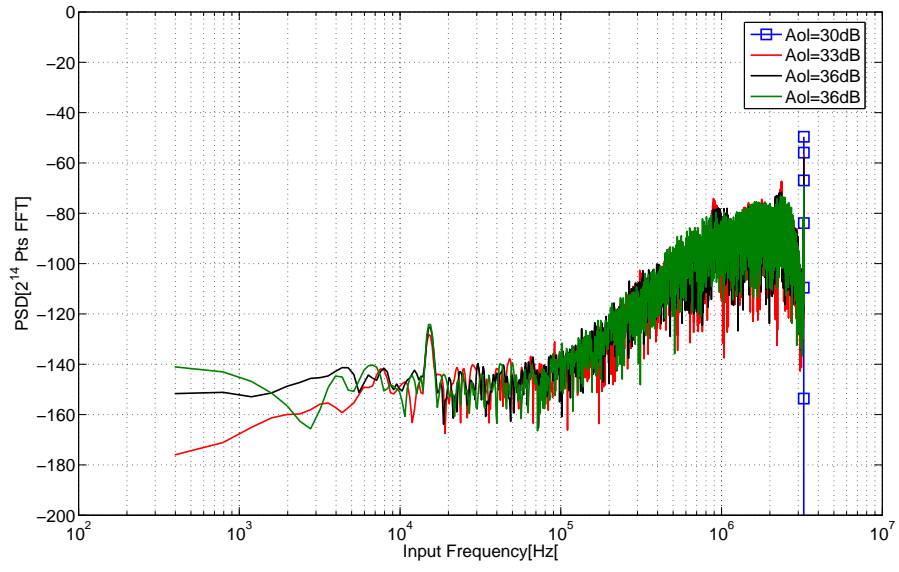


Figure 5.7: Output spectrum for third order topology and various values of amplifier open loop gain

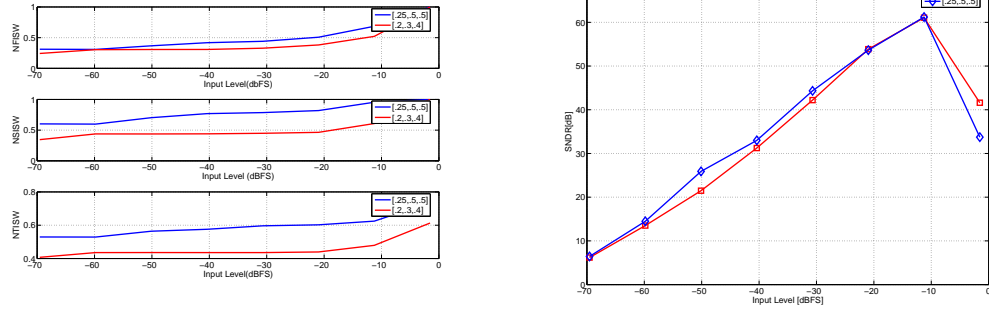


Figure 5.8: Integrator Swings(left) and Signal to Noise and distortion ratio third order designs with different loop filter coefficients

order modulator, with loop coefficients $[.25,.5,.5]$ for varying amplifier gain. Gain values as low as 34dB are tolerated. We therefore decided to increase the modulator order to 3 in order to keep the specification on amplifier open loop gain below 40dB. We resorted to the developed MATLAB simulation environment also to predict the converter peak signal-to-noise and distortion ratio(SNDR) for the $[.25,.5,.5]$ loop as a function of open loop gain. The result is shown in figure 5.9 and shows that SNDR values in the order of 60dB are realizable for an amplifier open loop gain of only 40dB. Even though the performance could be increased by using higher gain, going beyond 40dB would probably require the use of a 2-stage amplifier, which has a significant cost in power. Since a 6dB difference between dynamic range and peak SNDR is usually regarded as acceptable in the literature, we decided to tolerate the SNDR degradation. The loop filter coefficients were chosen to be $[.25,.5,.5]$ as in [45]. According to published data ([26]), a better choice would be $[.2,.3,.4]$. Figure 5.8 show the integrator output swings and the the SNDR versus input frequency for both choices. It shows that the choices yield almost equivalent peak SNDR(1.5dB improvement for the choice in [26]) for the values of parameters in the design; moreover, we found that when a $[.2,.3,.4]$ loop filter is chosen, higher amplifier gain is necessary to suppress limit cycles and avoid thresholding effects for small inputs.

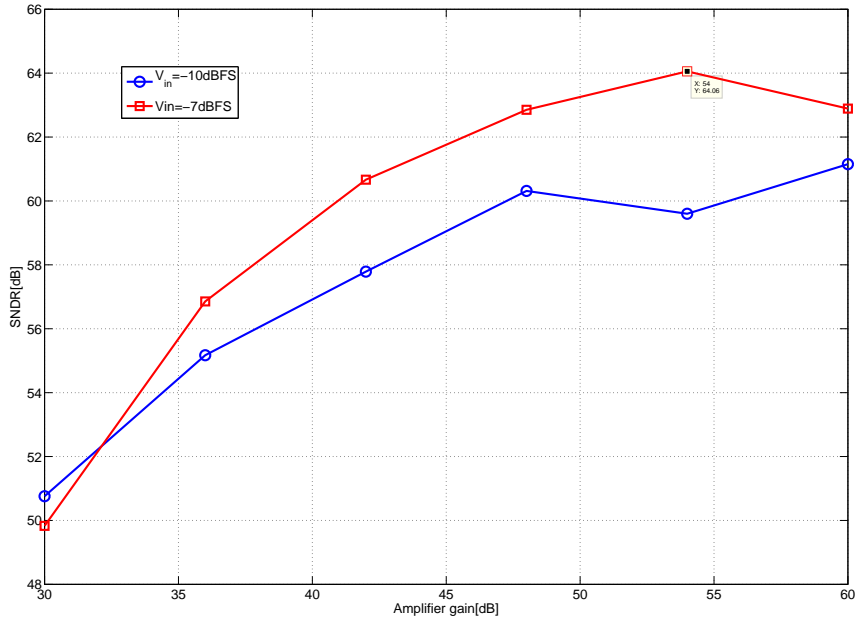


Figure 5.9: Signal to Noise and Distortion ratio of third order modulator versus amplifier open loop gain

5.6 Circuit Design

5.6.1 Sampling Network

To avoid sampling distortion and guarantee wide input sampling, a bootstrapped sampling circuit was used. Since this circuit was already described in chapter 4, the reader is referred to that chapter and to the reference [29] for the description of its operation.

5.6.2 Integrator design and optimization

The widely accepted rules of thumb for low-power, low-voltage operational amplifier design are to maximize signal swing and reduce as much as possible the

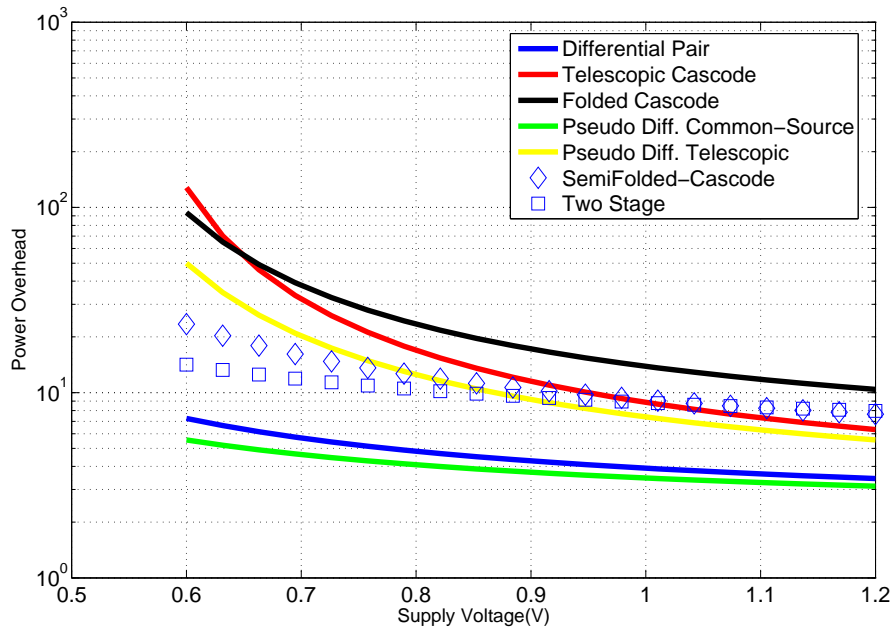


Figure 5.10: Amplifier Scaling analysis in the slew limited regime

number of stages¹. Since the number of stages is usually dictated by required open loop gain, open loop gain should also be minimized. These considerations are well summarized by the results of the amplifier scaling analysis performed in chapter 3, reproduced here in figure 5.10 for convenience. The analysis indicated that a differential pair single-stage amplifier would give 30 to 100% better power efficiency than a two stage amplifier, when only thermal noise is a concern. If single stage amplifiers with rail-to-rail swing were used, a much larger power benefit would result. In this context, we'll extend the results to include flicker noise, which is a major contributor to the overall noise budget for small sampling frequencies. We first review the equations describing noise in a sampled-data integrator.

¹In light of the results of [46], the second part of the rule seems only to hold for switched capacitor converters

Noise in an SC integrator

We distinguish between sampling noise and operational amplifier noise. For sampling noise, the well known formula

$$N_S^2 = \frac{2KT}{C_s} \quad (5.11)$$

holds for input referred noise, where the 2 takes into account differential operation. For operational amplifier noise, we used the expression

$$N_{o,OA}^2 = \frac{KT}{2G_m R_{sw} + 1} \left(\gamma \left(1 + \frac{C_I}{C_T} \right)^2 + 2G_m R_{sw} \left(\frac{C_I}{C_T} \right)^2 \right)$$

for output referred, which once multiplied by $(C_I/C_S)^2$ and referred to the input becomes

$$N_{OA}^2 = \frac{2KT}{C_{Leff} \cdot 2G_m R_{sw} + 1} \left(\gamma^* \left(\frac{C_T}{C_S} + \frac{C_S}{C_I} \right)^2 + 2G_m R_{sw} \left(\frac{C_T}{C_S} \right)^2 \right) \quad (5.12)$$

Where $C_T = C_p + C_S$ is the sum of the operational amplifier parasitic capacitance and the explicit sampling capacitance, and γ^* is the equivalent noise resistance-transconductance product of the amplifier and summarizes effects due to device bias point and integrator topology, Usually $G_m R_{sw} \ll 1$ so that the first term dominates. If one further neglects parastic capacitors $C_T \approx C_S$ and 5.12 reduces to a well known formula. Consider $V_{IRN}^2 = N_S^2 + N_{OA}^2$ and notice that we calculated noise variances for the $[0, F_s/2]$ bandwidth. For thermal noise, over a narrower bandwidth F_B , $V_{IRN}^2(F_B) = V_{IRN}^2(F_s) \frac{F_B}{F_s} = V_{IRN}^2(F_s) \frac{1}{OSR}$. This is a fundamental equation in $\sigma - \delta$ modulator design, as it can be directly used to calculate the sampling capacitors size once oversampling ratio and amplifier equivalent noise resistance are known. This equation will however only be accurate if the bandwidth and the sampling frequencies are low enough that flicker noise is negligible, and provide very inaccurate results at low frequency. To include the effect of flicker noise, we express the (continuous-time) power spectral density of the input referred noise of the amplifier as $N_I(f) = 4KT\gamma^* \left(1 + \frac{f_k}{f} \right)$. Integrating between f_1 and f_B , the variance of the noise contained in this band is $N_I^2(f_1, f_B) = 4KT\gamma^* \left(F_b + f_k \log \left(\frac{F_B}{f_1} \right) \right)$. Expressing in terms of V_{IRN}^2 (the total

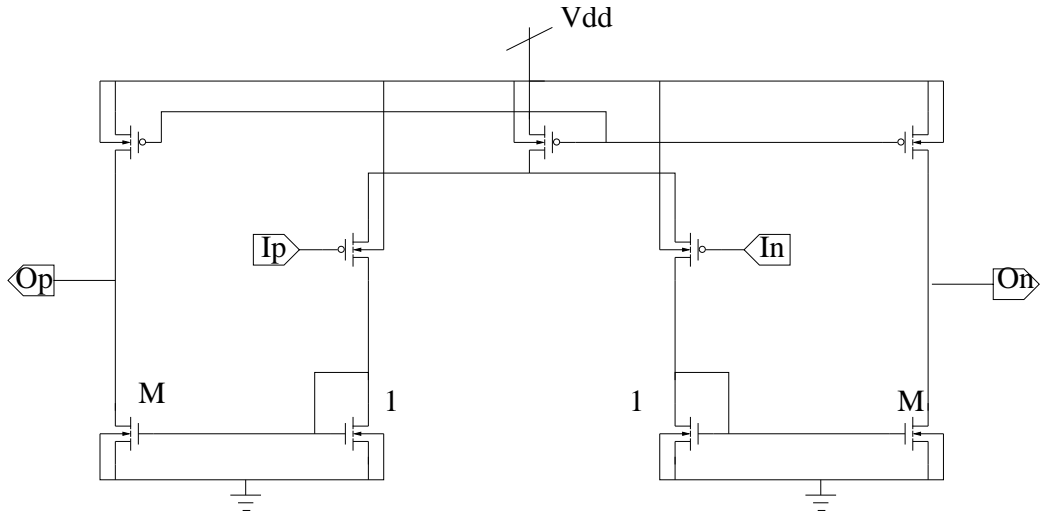


Figure 5.11: Amplifier topology used in [26] with removed output stage

thermal noise in the $[0, F_s/2]$ band), we get to ²

$$V_{IRN}^2(F_B, f_1, f_k) = V_{IRN}^2\left(\frac{F_B}{F_S}\right)\left(1 + \frac{f_k}{F_B} \log\left(\frac{F_B}{f_1}\right)\right) \quad (5.13)$$

Assuming $f_1 = 100Hz$ In order for flicker noise not do dominate the budget (i.e. $\frac{f_k}{F_B} \log\left(\frac{F_B}{f_1}\right) \leq 1$, we need $f_k \leq 18KHz$, which requires careful design.

Amplifier design considerations in the presence of flicker noise

Because of excellent experimental results reported, we started transistor-level design with the topology described in [26]. This topology (See figure 5.11) has a class-AB output stage, and a current-mirror based input stage. We show that this topology presents a noise-stability tradeoff that is unfavorable in low-frequency designs. Consider devices $M3$ and $M4$ in figure 5.11. Their channel noise directly adds to the total amplifier noise; also, called K the ratio of width of $M7$ to the width of $M3$, the $M7$ - $M3$ current mirror introduces a non dominant pole in the amplifier frequency response, that is placed at $f_{nd} \approx \frac{f_t^{(M3)}}{M+1}$. For stability reasons, this pole should be located at a frequency at least twice as high as the integrator

²Rigorously, we should include a factor χ equal to the ratio of thermal noise from the op-amp to total thermal noise in front of the second term. This is neglected here for brevity

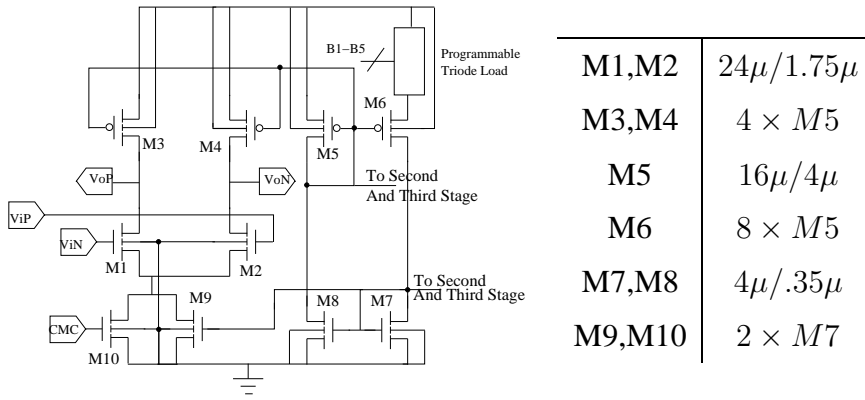


Figure 5.12: Schematic and sizing of first amplifier

unity-gain bandwidth UGF. Therefore, the resulting set of constraints on M3 is

$$\begin{aligned}
 f_k &\leq \frac{F_B}{\log\left(\frac{F_B}{f_1}\right)} = 18KHz \\
 f_t &\geq 2UGF(M+1) \approx 10F_S(M+1) \\
 \frac{f_t}{f_k} &\geq 2UGF(M+1) \frac{\log\left(\frac{F_B}{f_1}\right)}{F_B} \approx 40 \cdot OSR \cdot (M+1) \log\left(\frac{F_B}{f_1}\right) \quad (5.14)
 \end{aligned}$$

Equation 5.14 imposes a *minimum* ratio of transition frequency to corner frequency, which should be compared with the limitation stated in chapter 3 and in [47] for the *maximum* ratio available for the process in the subthreshold regime. At $F_B = 50KHz$, f_1 and $OSR=64$, we get $\frac{f_t}{f_k} \geq 8000(M+1)$. Although simulation data show this value is reachable in this process, calculations showed that it would not be achievable. In the absence of any data on the model accuracy for long channel devices, we chose to revert to a different topology to reduce flicker noise. The chosen amplifier topology is shown in figure 5.12 and trades off swing for flicker noise performance. The load devices do not contribute non-dominant poles, so that their size can be chosen for flicker noise independently from stability considerations. The non-dominant pole, as described in [48], is set by the non-quasi-static behavior of the input transistors, and is approximately located at $5f_t$. For the same phase margin and noise performance, the required transition frequency to flicker corner ratio becomes therefore $\frac{f_t}{f_k} \geq 4 \cdot OSR \cdot \log\left(\frac{F_B}{f_1}\right) \approx 600$, which is easily reachable. The potential reduction in flicker noise offsets the reduction in swing coming from the presence of a tail current source. Assuming $V_{dsat} = 125mV$ we find $V_o^{(Max)} = 525mV$, $V_o^{(Min)} = 225mV$, so that the inte-

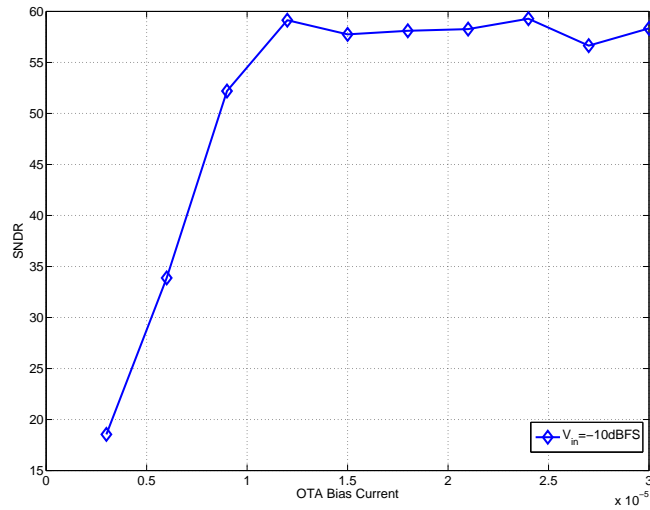


Figure 5.13: Simulated Performance Versus OTA Bias Current

grator output is .3V 0-Peak. Setting $V_{ref} = .3V$ a minimum detectable signal of -70dBFS=100uV requires an input referred noise less than $6nV^2$. If we assume thermal and flicker noise to contribute the same to the total budget, $N_{th} \leq 3nV^2$ is required, which using equation 5.12 is translated into a 500fF sampling capacitor. The long PMOS output devices($64\mu/4\mu$) are sized to give a negligible contribution to the amplifier flicker noise, while introducing only a small parasitic capacitance at the output.

The analysis on settling optimization presented in chapter 3 is used to size the input devices $24\mu/1.75\mu$ to achieve a 10KHz flicker noise corner and achieve a good tradeoff between transconductance efficiency, input common mode range and open loop gain. The DC bias current and transconductance of the amplifier were determined through behavioral simulations (See Fig.5.13) to respectively have nominal values of $16\mu A$ and $144\mu S$, corresponding to a nominal slew rate of $20MV/s$ and a gain bandwidth product of $30MHz$.

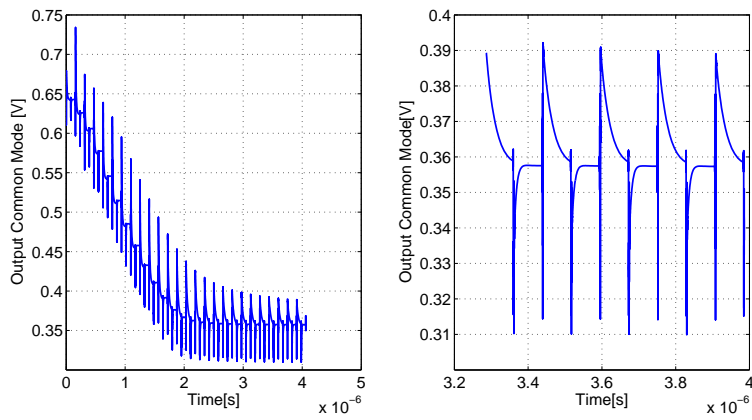


Figure 5.14: Simulated First Integrator Common Mode : Settling(left) and steady state detail(right)

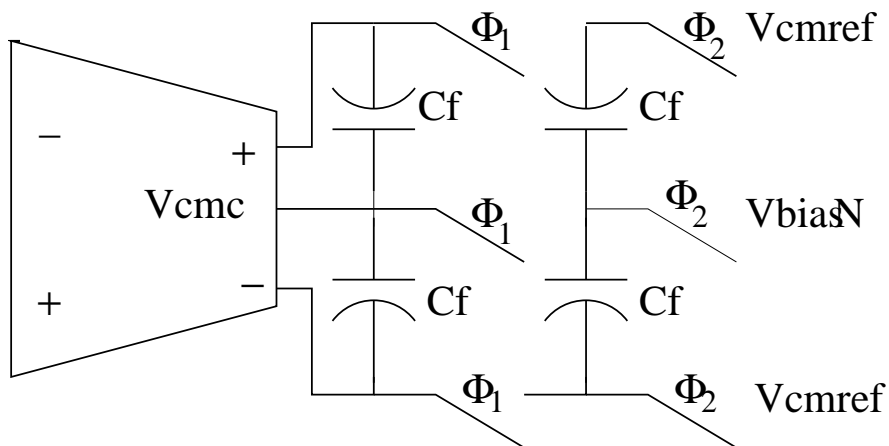


Figure 5.15: Dynamic Common Mode Feedback

Common Mode Feedback

A standard sampled-data common-mode feedback was used in this design(See figure 5.15 and also [49]). The common-mode sampling-capacitors C_{f1} and C_{f2} were set to 50fF to minimize loading to the differential mode circuit, while ensuring low-loss by charge redistribution with the gate capacitance of M10. A simulated output common mode waveform for the first integrator is shown in figure 5.14.

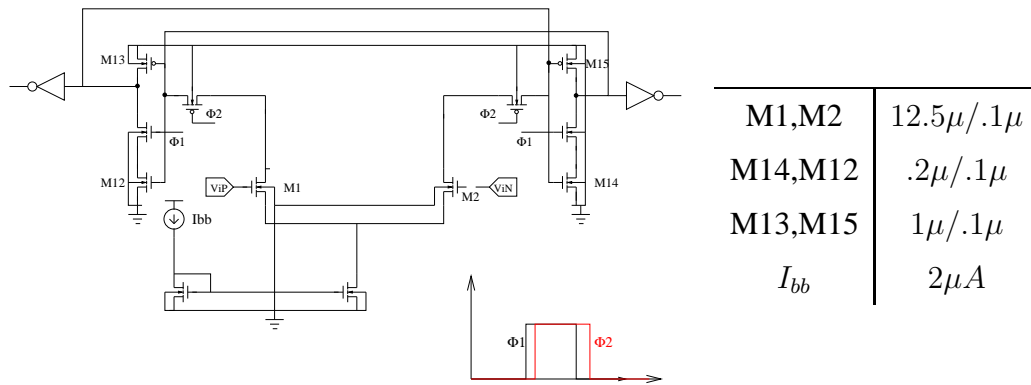


Figure 5.16: Comparator Schematic and sizing

5.6.3 Second and Third Integrators

Being their non-idealities suppressed by the gain of the integrator, the second and third integrators are not critical and can therefore be scaled. We simultaneously scaled scaled sampling capacitors, bias current and device widths by a factor of 4, leaving device lengths unvaried.

5.6.4 Comparator

Comparator performance is also not critical([44]). An annotated schematic of the circuit used is shown in figure 5.16. For the operation, the reader is referred to the previous chapters.

5.6.5 Clock Generation and distribution

The modulator uses a conventional bottom-plate sampling scheme. The circuit in figure 5.17 is used to generate the 2 non-overlapping phases $\Phi 1$ and $\Phi 2$ as well as their early versions $\Phi 1A$ and $\Phi 2A$.

All the integrators operate as half-delaying(LDI) integrators; so that in order to ensure correct implementation of a prototype transfer function specified using full-delaying integrators equalizing delays have to be inserted in the feedback

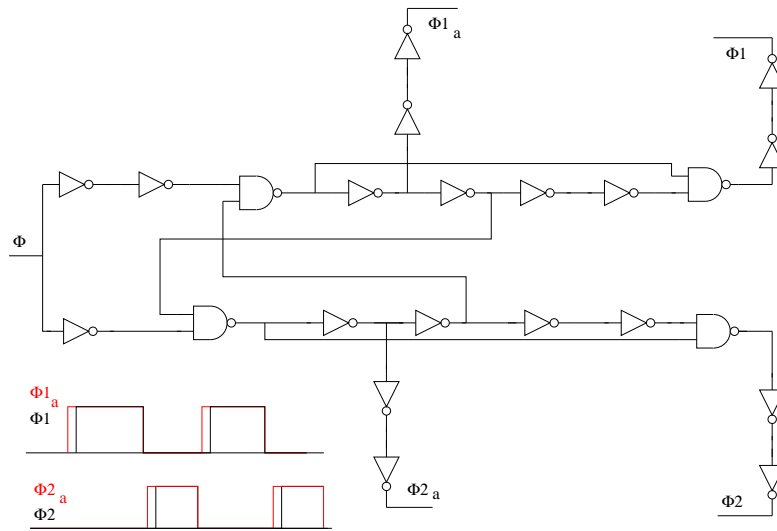


Figure 5.17: Non-overlapping clock generator

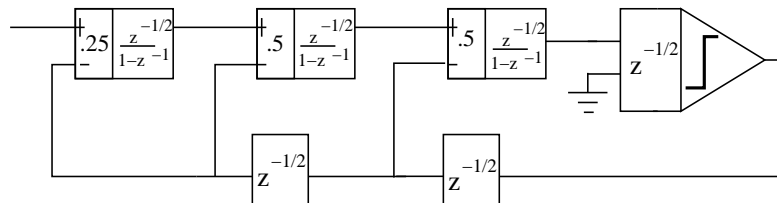


Figure 5.18: Modulator Architecture

path [45]. These delay elements are simple flip-flops that resample the DAC control signal of selected stages with the correct polarity; their collocation and timing are shown in figure 5.18.

5.6.6 Bias Circuits and programmability

The bias currents in the amplifiers can be changed in 31 steps in range between $I_{nom}/10$ and $3I_{nom}$ by a digitally controlled supply-independent current source (See Fig.5.19) where PMOS transistors are used as current-defining elements instead of polysilicon resistors to minimize area. As a result of this choice, the output current is not PTAT, but instead (to first order) temperature independent for

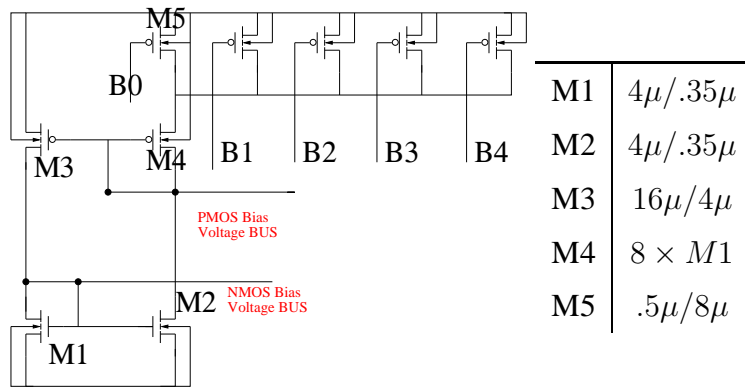


Figure 5.19: PTAT Bias circuit and sizing

the chosen parameter values. Bias is distributed throughout the die in the voltage domain. The current flowing in each branch of the biasing circuit is in a ratio 1:4 with the nominal tail current of the first operational amplifier, and hence in a ratio 1:1 with the tail current of the second and the third amplifiers. The power consumption of this bias circuit is .

5.7 Chip Floorplan and layout

A die photograph is shown in figure 5.20. The operational amplifiers occupy the center strip of a $370\mu m \times 300\mu m$ area. Most of the area is taken by the integrating and sampling capacitors, for which a MIM layer was used. To save space and minimize parasitics, all the sampling switches are placed underneath the capacitors they are connected to. Since $\Sigma - \Delta$ modulators are known to be rather insensitive to mismatch, centroiding technique were not used in this layout. Instead, special care was taken in routing the clock lines in such a way that they would interfere minimally with the signal lines.

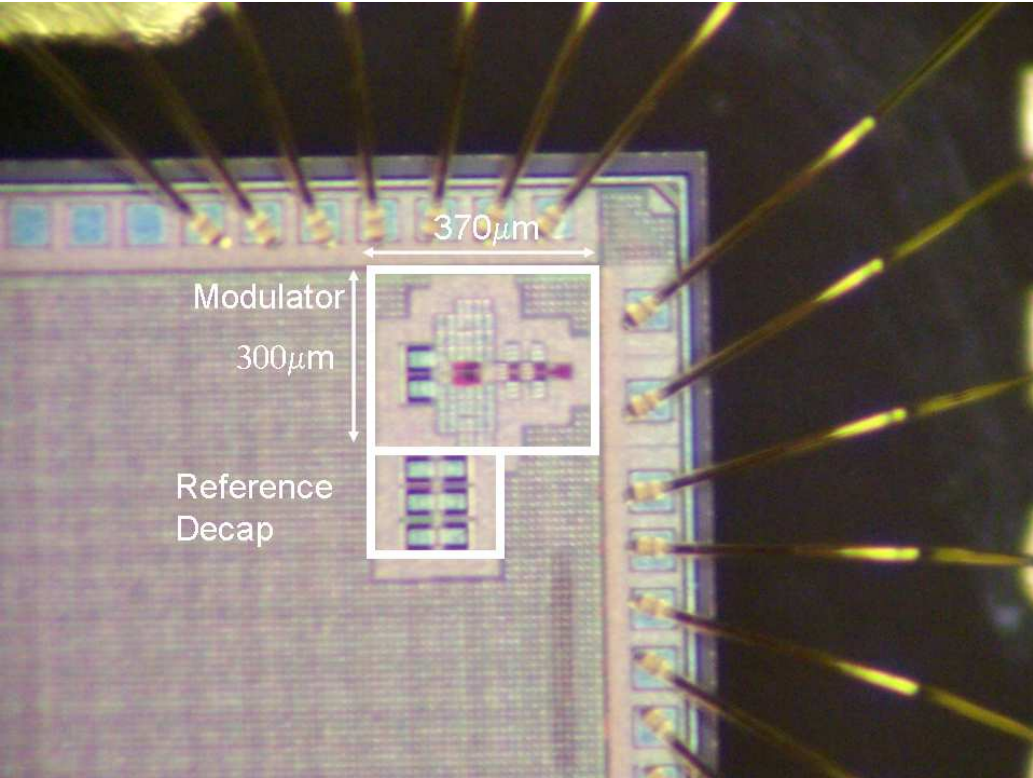


Figure 5.20: Chip photograph

5.8 Experimental Results

5.8.1 Test Setup

Due to size constraints, the die was mounted on a custom designed board using chip on board(COB) assembly. Single ended input signals generated from the instrumentation and filtered off-board were converted to differential by an on-board low noise ADI8139 driver. The reference voltages are generated on the board by an adjustable output low noise reference generator(LM4121) and buffered by another ADI8139 driver. Chip outputs are read-back using a logic analyzer. Two different samples were characterized, showing closely matching performance.

5.8.2 Single tone tests

The modulator output for shorted input terminals is shown in figure 5.21. No spurious tones are present. Figure 5.22 displays SNDR and SNR versus input amplitude (normalized to the .3V full scale). The peak SNDR is 59.5dB, while the peak SNR is 61dB. A minimum detectable signal of $100\mu V$ is measured. Figure 5.23 displays the output spectrum for input of 125mV, corresponding to the peak SNDR of 59.5dB. A Spurious Free Dynamic Range (SFDR) of 63dB is measured, limited by third order distortion from integrator nonlinear gain. As apparent from figure 5.22, the measured results match very closely the behavioral simulations performed in MATLAB, validating our design methodology.

5.8.3 Interference Rejection

As mentioned above, one of the potential advantages of using $\Sigma - \Delta$ modulation to perform analog-to-digital conversion lies in the reduced amount of filtering required by this architecture. This is only possible ([50]), if the out-of-band signals do not interact with the converter noise shaping characteristic, increasing the in-

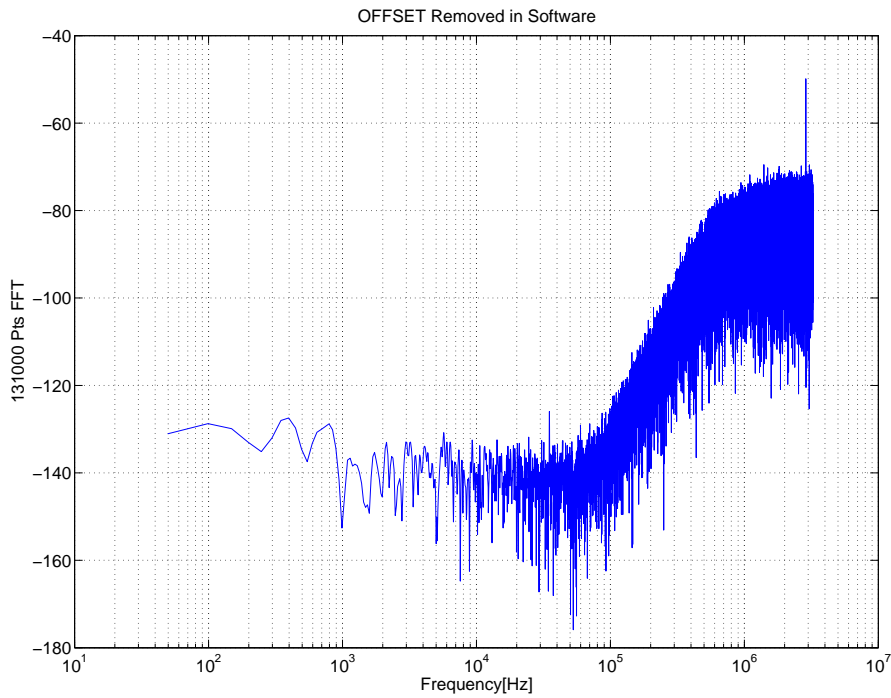


Figure 5.21: Modulator noise floor with shorted inputs. The flicker noise corner is approximately 10KHz; no spurious tones are present.

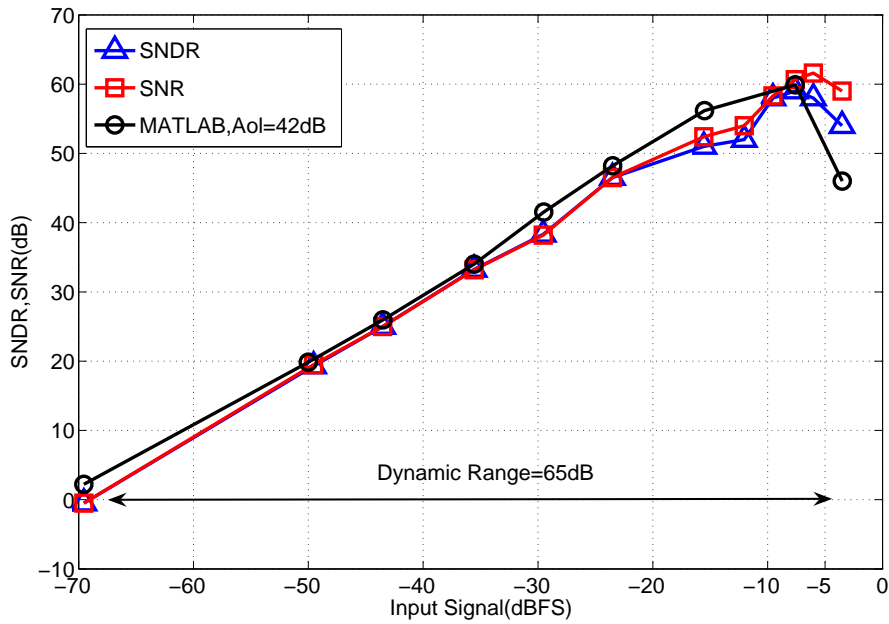


Figure 5.22: Signal to noise and distortion ratio versus input level

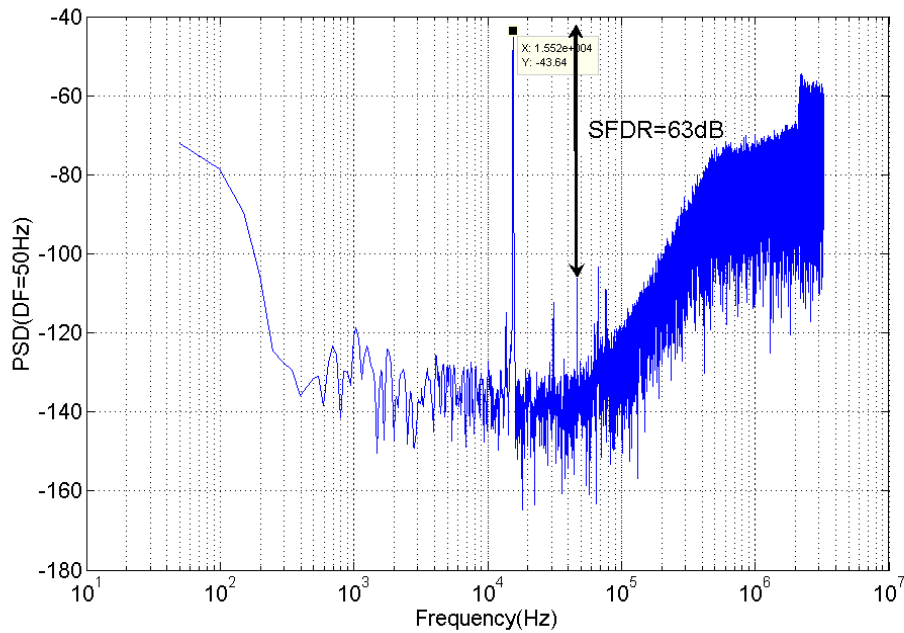


Figure 5.23: Output spectrum for -7dBFS input. The tones at 52KHz and 75KHz are caused by instrumentation noise pickup.

band noise and ultimately reducing sensitivity. Although interference robustness was not explicitly considered in the converter design, this data is seldom reported for modulators in the literature (with the important exceptions of [50], [51]) and constitutes useful information on the performance of the standard feedback architecture in this respect. To measure desensitization due to out of band interferer, we apply a large out of band tone and measure the variation in the in band noise floor. The results are reported in figure 5.24. We can highlight two important facts: first, a certain amount of desensitization is present even for rather small interferer amplitudes. The amount of desensitization is however limited to 2-3dB even in the case of a close-in 300KHz interferer. Second, the amount of interference that can be applied to the converter until a certain fixed degradation in in-band performance occurs, depends strongly on the input frequency. This behavior reflects the low-pass nature of feedback loop-filters topology.

Converter performance for pulse width modulated input signals, such as those expected at the output of a super-regenerative radio before analog demodulation, was also measured. A Wavetek166 function generator was used to produce the

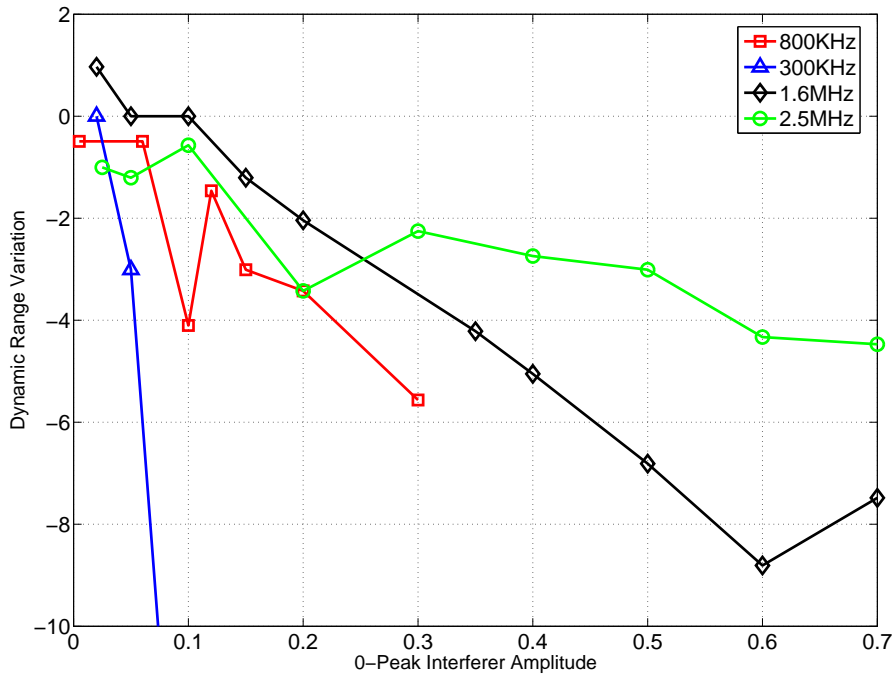


Figure 5.24: Measured converter desensitization due to out-of-band blockers

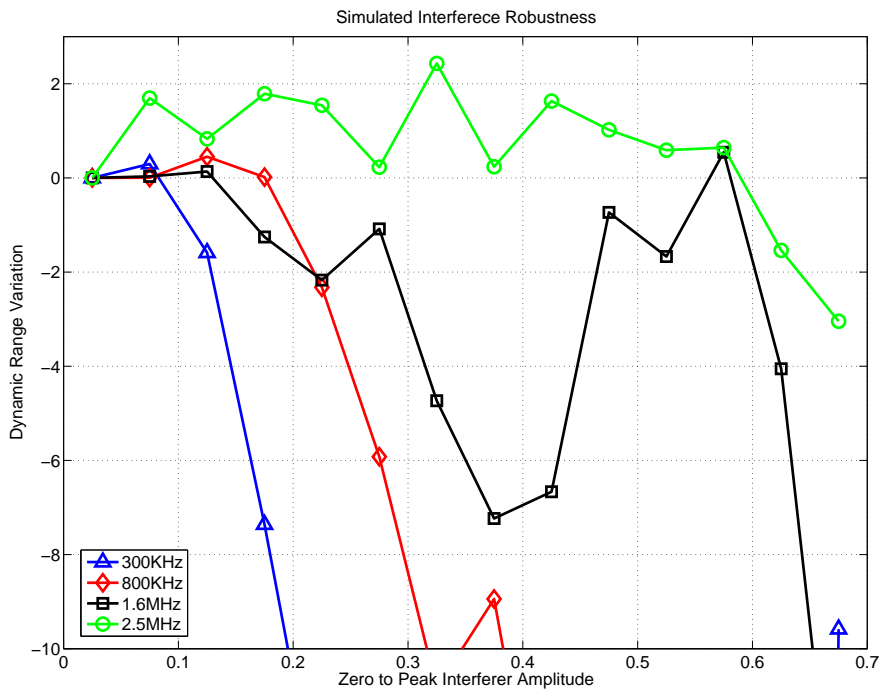


Figure 5.25: Simulated converter desensitization due to out-of-band blockers

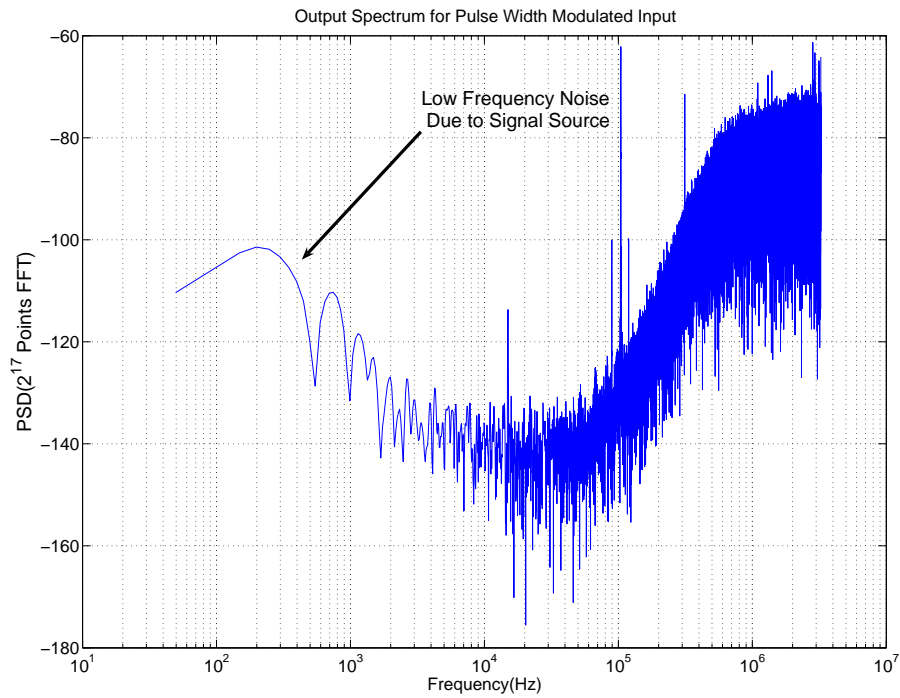


Figure 5.26: Measured output spectrum for pulse-frequency modulated input signal

square-wave signal with 100KHz nominal frequency, and a Rhode and Schwarz sinusoidal signal source was used to externally modulate its period with a frequency of 15KHz. Due to the high low-frequency noise content of the sinusoidal source, the measurement only has qualitative meaning. The output spectrum is shown in Fig.5.26 The measurement shows that the converter remains stable under the measurement conditions; SNDR measurement is however meaningless in this setup. A summary of the measured performance is reported in table 5.27.

5.9 Conclusions and comparison with literature

We developed a methodology for the design of low-voltage, low-power $\Sigma - \Delta$ converters, and applied it to the design of a low-power modulator for wireless sensor network receivers. The methodology allows successful minimization

Signal Bandwidth	50KHz
Peak SNDR	59.5dB
Peak SNR	61dB
Dynamic Range	65dB
SFDR	63dB
Clock Frequency	6.5MHz
Power Dissipation	$27\mu W$
Power Supply	0.65V

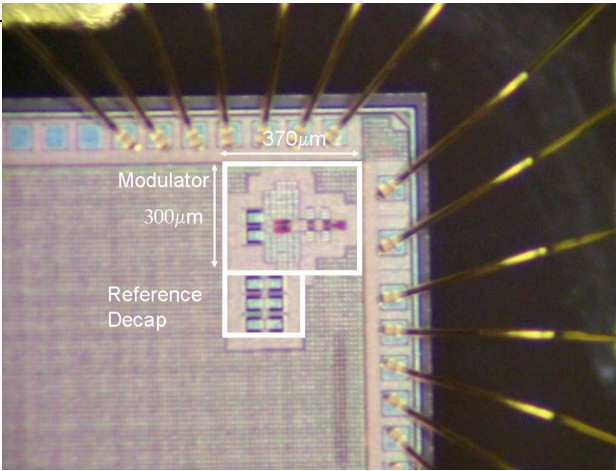


Figure 5.27: Converter Performance Summary

Ref.	DR[dB]	SNDR[dB]	BW[Khz]	V_{dd} [V]	FOM [pJ/Conv]	FOM_{noise}	Power [μW]
[52]	74	74	24	.5	1.63	35e-6	300
[45]	77	62	16	.9	1.2	330e-6	40
[53]	75	67	8	.7	2.8	52-6	80
[54]	83	80	10	.9	1.22	166e-6	200
[42]	78	78	20	.6	2.36	25e-6	1000
[26]	88	83	20	1	.31	1.66e-3	130
This work	65	59.5	50	.65	.36	122e-6	27

Table 5.1: Comparison with other low-voltage $\Sigma - \Delta$ converters

of amplifier specifications for a given converter linearity requirement, resulting in power efficient designs. The experimental modulator reaches a state-of-the-art power/performance ratio, despite the low operating voltage(See Tab.5.1).

Chapter 6

Conclusions and final considerations

In this work, we have shown a complete design methodology to design low and moderate resolution ultra-low power analog to digital converters; as well as experimental results validating this methodology.

The proposed converters meet the performance requirements of wireless sensor network radios, and show that complete ultra-low-power radio receivers can be realized for less than $100\mu W$ [35]. While these works are distinguished by low operating supply and low power in an absolute sense, the power efficiency achieved compares favorably with literature, as summarized in table 6.1. In this table, some of the calculated values of power consumption, already reported in chapter 2 are also reproduced. Apparently, the power efficiency achieved in this work is still far from the calculated values.

For the SAR converter cases, the overhead power is due to two main factors: first, the estimate did not include digital power, which represents the largest contributor of power dissipation in all implementations. An optimized, custom design of the digital logic would reduce this contribution, easily increasing power efficiency. Second, generating on chip bias currents smaller than $1\mu A$ requires large resistors and is impractical from the perspective of area consumption. The comparators therefore have power dissipation and speed exceeding their requirements, as verified experimentally also in this work (See chapter 3). This results in analog power

Arch.	Resolution (ENOB @ $F_s/2$)	F_s	Power	Input Cap.	V_{dd}	FOM (pJ/conv)
SAR	8b	100KS/s	$.25\mu W$	$1.28pF$	1V	.009
[25](SAR)	8b(4.5b)	100KS/s	$3\mu W$	$3pF$	1V	1.2
SAR	6b	1.5MS/s	$.4\mu W$	$320fF$.5V	.004
This work, Ch.3	6b(5.5b)	1.5MS/s	$14\mu W$	$310fF$.5V	.2
This work, Ch.4(Core)	6b(4.8b)	1 MS/s	$6\mu W$	$310fF$.5V	.23
$\Sigma - \Delta$	11b	100KS/s	$10\mu W$	$65fF$.65V	.029
This work,Ch. 5	10.5b(9.55b)	100KS/s	$27\mu W$	$500fF$.65V	.3
$\Sigma - \Delta$	14b	40KS/s	$147\mu W$	$220fF$	1V	.22
[26]($\Sigma - \Delta$)	14b (12b)	40KS/s	$140\mu W$	$6pF$	1V	.22
SAR	12b	100KS/s	$1.6\mu W$	$180pF$.5V	.004
[27](SAR)	12b(10b)	100KS/s	$25\mu W$	<i>n.r.</i>	1V	.165

Table 6.1: Comparison of this work to published results and estimated performance metrics. Notice that *forall* converters, the figure is reported as $P_d/ENOB/F_s$, where ENOB is measured at Nyquist input.

dissipation higher than necessary. As suggested in other parts of the work, a higher sampling frequency would allow to take more effectively advantage of the technology intrinsic speed, guaranteeing better power efficiency. This indicates that even higher values of power efficiency are likely to be achieved using this architecture than what is reported here.

The measured performance of the prototype oversampling converter is within one order of magnitude of the estimated one. In the design described in this thesis, the second and the third stages of the converter, and the bias circuit, consume together as much power as the first operational amplifier. It seems hence obvious that a converter with fewer stages would have dissipated lower power. Unfortunately, reducing the number of stages makes limit cycles more likely to occur, and consequently calls for higher amplifier gain.

In general, for $\Sigma - \Delta$ converters, the bounds on power efficiency seem therefore

to be tighter, and the room for improvement smaller. Even under these circumstances, the adoption of a continuous-time loopfilter might improve power efficiency by as much as factor of 3.

Progressing down the road of scaling, successive approximation converters are bound to keep improving their performance and their power efficiency; ever-cheaper digital circuits can be used to extend the accuracy beyond the limits imposed by components mismatch([55], [56]). They are therefore candidate to replace pipelined converters, which present much more challenges in scaling.

Despite the increase in power efficiency however, this thesis shows that obtaining absolute low-power operation is becoming more and more challenging at low-speeds due to the increased leakage currents of digital blocks, as well to the increased significance of traditionally non-critical blocks, such as the reference generator and buffer. An elegant solution to this problem is to use a fully-asynchronous ADC, as proposed in [57], that performs the computation as fast as possible, delivers the output and shuts down.

$\Sigma - \Delta$ converters, especially as continuous-time implementations reached maturity, have also started to conquer space in specification domains that used to belong to pipelined converters([46]). As switching speed increases, the amount of oversampling that can be applied increases, enabling wider bandwidths or higher resolution. With clock frequencies already breaking the gigahertz barrier, long-dreamed concepts such as RF-digitization might soon appear.

Similarly to the previous case however, low-power, low frequency applications will suffer from the increased leakage of future technologies. Similarly to pipelined converters, most high-resolution $\Sigma - \Delta$ converters require an operational amplifier. Even if performance requirements of this amplifier, as demonstrated in this thesis, are very relaxed compared of those typical of Nyquist-rate converters, scaling of this block will be critical. An interesting solution is presented in [50], where the linearity and the dynamic range specifications of the converter are separated, and a merged filter/A/D converter is realized. The ADC obtains a peak SNDR of 55dB across variable full-scale ranges, so that the operational amplifier specifications are relaxed. Although this strategy is viable in radio-receivers, it might not result portable to other applications. In these cases, alternative ways of implementing

the integrators, such as passive switched capacitor circuits or the realization of a phase-domain integrator as a VCO [58], might become the preferred choice.

Appendix A

Linearity Analysis of a Trit-Based DAC

The analysis will be carried out in the charge domain for ease of computation.

The digital to analog converter considered is composed of two independent capacitor arrays, $C_P^{(i)}, i = 1 \dots 2^{N-1} - 1$ and $C_N^{(i)}, i = 1 \dots 2^{N-1} - 1$; for differential symmetry,

$$C_N^{(i)} = C_P^{(i)} = C_0 \quad (\text{A.1})$$

for the nominal values. Due the influence of process variations, the capacitor values are better modeled as independent identically distributed (i.i.d.) gaussian random variables with mean given by A.1 and variance given by Eq.

$$\sigma^2(i) = \sigma^2(C_0) \quad (\text{A.2})$$

. Assume positive codes only are allowed, so that MSB=1 and we only need to focus on the N-1 remaining bits(magnitude code). To encode the output level i , $C_P^k, C_N^k, k = 1 : i - 1$ are tied to respectively V_{RH} and V_{RL} , while $C_P^k, C_N^k, k = i : L = 2^{(N-1)} - 1$ are tied to V_{cmR} . The resulting differential charge is $Q_d(i) = \sum_{k=1}^{i-1} (C_P^k \cdot V_H - C_N^k \cdot V_L) + \sum_{k=i}^L (C_P^k - C_N^k) V_{cm}$. To calculate linearity, the end point line(EPL) is needed. This is expressed as

$$\sum_1^L (C_P^k \cdot V_L - C_N^k \cdot V_H) + (V_H - V_L) \sum_1^L \frac{(C_P^k - C_N^k)(i + L)}{2L} \quad (\text{A.3})$$

Note that due to the sign-magnitude coding, $2L$ levels are realized, as opposed to $2L - 1$. To further simplify the derivations, we assume $V_H = V_{dd}, V_L = 0, V_{cm} = V_{dd}/2$. The integral non linearity (INL) can be expressed as $INL(i)/V_{dd} = (Q_d(i) - EPL(i))/V_{dd} = \sum_k^{i-1} C_P^{(k)} + \frac{1}{2}(\sum_i^L (C_P(k) - C_N^{(k)}) + \sum_1^L C_N^{(k)} - \frac{1}{2}(\sum_1^L (C_P(k) - C_N^{(k)}) - \frac{i}{2L}(\sum_1^L (C_N^{(k)} + C_P^{(k)}))$. To compute the variance, we need to separate contributions from independent variables, as they will add in power. After some algebra,

$$INL(i)/V_{dd} = [(\frac{1}{2} - \frac{i}{2L}) \sum_{k=1}^{i-1} C_N^{(k)} - \frac{1}{2}(\sum_{k=1}^L C_N^{(i)})] + [(\frac{1}{2} - \frac{i}{2L}) \sum_{k=1}^{i-1} C_P^{(k)} - \frac{1}{2}(\sum_{k=1}^L C_P^{(i)})]$$

and finally

$$INL(i) = [-\sum_{k=1}^L C_N^{(k)} \frac{i}{2L} + \sum_{k=1}^{i-1} C_N^{(k)} (\frac{1}{2} - \frac{i}{2L})] + [-\sum_{k=1}^L C_P^{(k)} \frac{i}{2L} + \sum_{k=1}^{i-1} C_P^{(k)} (\frac{1}{2} - \frac{i}{2L})] \quad (A.4)$$

The variance can be expressed as

$$\sigma^2(i) = 2\sigma^2(-\frac{i^2}{4L}(\frac{L+1}{L}) + i\frac{L+2}{4L} - \frac{1}{4})$$

Differentiating with respect to i (treated here as a continuous variable), $i_{max} = \frac{L+2}{L+1} \frac{L}{2}$ is found. The corresponding variance is

$$\sigma_{Max}^2 = \frac{\sigma^2}{8} \frac{L^2}{(L+1)} \quad (A.5)$$

A behavioral model was built in MATLAB to verify the analysis. Figures A.1-A.2 show respectively INL of a single run and INL variance profile versus input code, and normalized maximum variance versus number of bits for a trit based architecture. These results follow closely analytical calculations showing that due to the reduced number of unit elements (half with respect to the case of a standard DAC), the variance of the INL is halved for the same unit element variance. This means that roughly a four-fold reduction and capacitance can be achieved, for comparable capacitive layer chosen. Although capacitor mismatch only has been considered so far, the case where $V_{cm} \neq \frac{V_H + V_L}{2}$ gives rise to further distortion. This can be evaluated by removing the assumption $V_{cm} = V_{dd}/2$ made in the previous section, obtaining

$$INL(i) = (\sum_{k=1}^{i-1} C_p^{(k)}) (\frac{V_H + V_L}{2} - \frac{V_H - V_L}{2} \frac{i}{L}) + \sum_{k=i}^{L-1} C_p^{(k)} (V_{cm} - \frac{V_H + V_L}{2} - \frac{V_H - V_L}{2} \frac{i}{L})$$

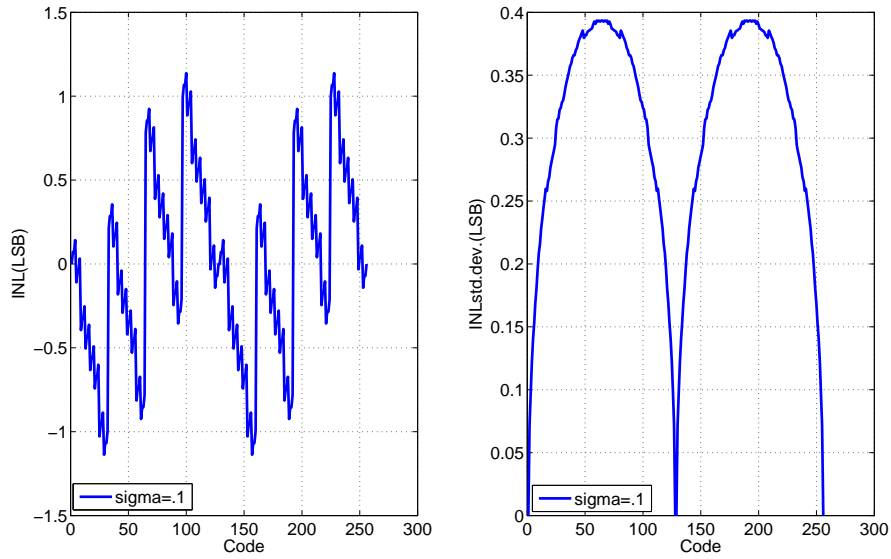


Figure A.1: INL results from a single run(right) and averaged standard deviation profile over 2000 runs. $\sigma = .1, B=8$ was assumed

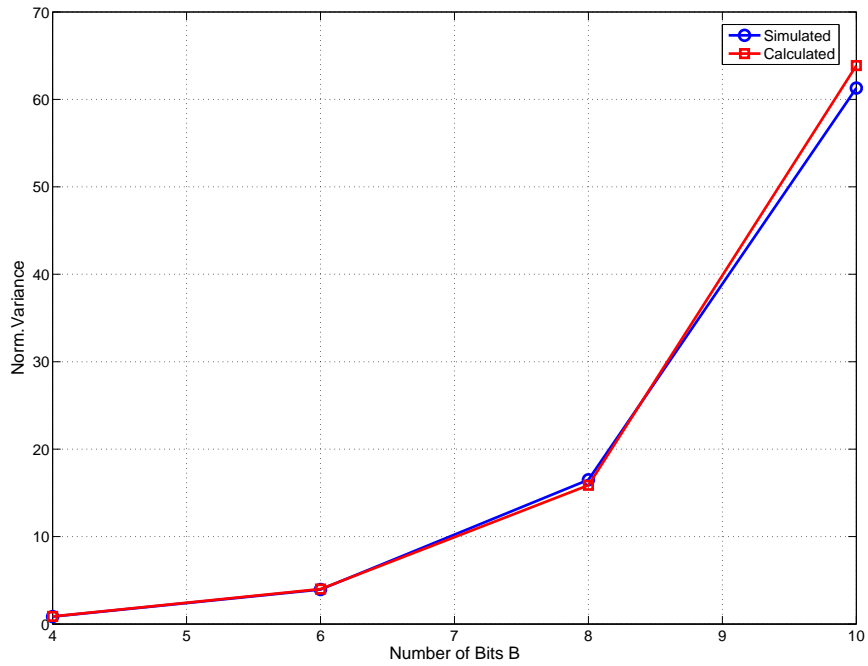


Figure A.2: Maximum INL variance(normalized to component mismatch σ) for different number of bits

from here, it can be seen that a term $V_{cm} - \frac{V_H + V_L}{2}$ is now added. This term will be small for codes close to the boundaries, but it will limit the linearity across zero.

Appendix B

Analysis of Capacitance Mismatch Induced offset in a regenerative latch

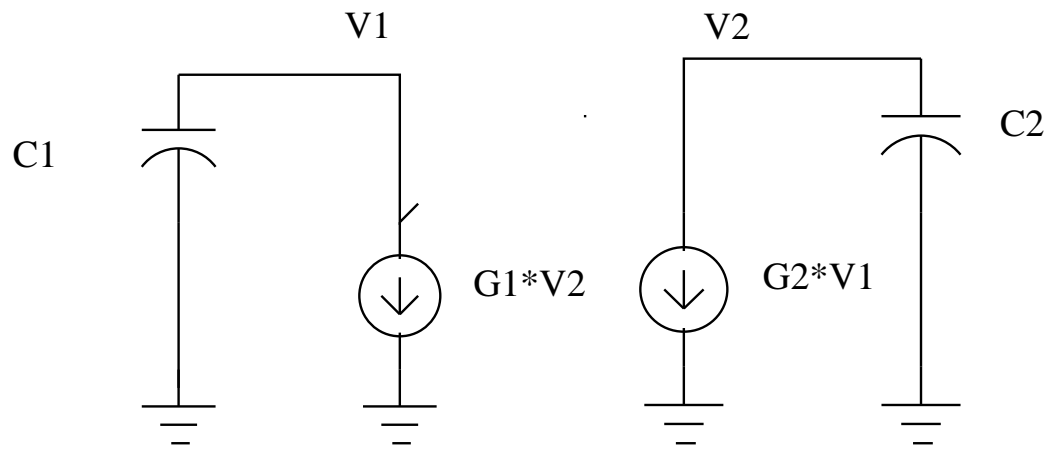


Figure B.1: Regenerative latch model used in the analysis

Consider the model of a regenerative latch shown in figure B.1. The differential equations for the voltages at nodes 1 and 2, called V_1 and V_2 read as in

B.20

$$C_1 \frac{dV_1}{dt} = -G_1(V_2) \quad (\text{B.1})$$

$$C_2 \frac{dV_2}{dt} = -G_2(V_1) \quad (\text{B.2})$$

Differentiating the first equation and substituting the second,

$$\frac{d^2V_1}{dt^2} = \frac{G_1G_2}{C_1C_2}V_1$$

is found, which admits a solution of the form

$$V_1(t) = A_{11}e^{-\frac{t}{\tau}} + A_{12}e^{\frac{t}{\tau}} \quad (\text{B.3})$$

Where B.4

$$\tau = \sqrt{\frac{C_1C_2}{G_1G_2}} \quad (\text{B.4})$$

holds. An identical differential equation may be derived for V_2 . The solution for V_2 reads as in B.5

$$V_2(t) = A_{21}e^{-\frac{t}{\tau}} + A_{22}e^{\frac{t}{\tau}} \quad (\text{B.5})$$

The constants A_{ij} depend on initial conditions; and A_{12} and A_{22} are of particular interest, since they represent the growing modes. Notice that, due to the cross coupling, the time constant of the growing modes is the same for V_1 and V_2 . The intuition that capacitive mismatch introduces offset by slowing down one side of the comparator is therefore incorrect. As shown in the following, the offset is introduced by modifications of the A_{ij} constants. To prove this statement, consider the system in presence of initial conditions $V_1(0) V_2(0)$. Due to the cross coupling, $\frac{dV_1}{dt} |_{0=} = -\frac{G_1}{C_1}V_2^*$. The following equations hold:

$$V_1^* = A_{11} + A_{12} \quad (\text{B.6})$$

$$\frac{dV_1}{dt} |_{0=} = \frac{+A_{11} - A_{12}}{\tau} = \frac{G_1}{C_1}V_2^* \quad (\text{B.7})$$

$$V_2^* = A_{21} + A_{22} \quad (\text{B.8})$$

$$\frac{dV_2}{dt} |_{0=} = \frac{+A_{21} - A_{22}}{\tau} = \frac{G_2}{C_2}V_1^* \quad (\text{B.9})$$

Defined $\chi = \tau \frac{C_1}{G_1} = \sqrt{\frac{G_2 C_1}{C_2 G_1}}$, the equations read

$$V_2^* = \chi(A_{11} - A_{21}) \quad (\text{B.10})$$

$$V_1^* = \frac{1}{\chi}(A_{12} - A_{22}) \quad (\text{B.11})$$

$$V_1^* = A_{11} + A_{12} \quad (\text{B.12})$$

$$V_2^* = A_{21} + A_{22} \quad (\text{B.13})$$

Because A_{11} and A_{21} represent decaying mode, we can eliminate them by using equations B.12, B.13 to obtain:

$$V_2^* = \chi(V_1^* - 2A_{21}) \quad (\text{B.14})$$

$$V_1^* = \frac{1}{\chi}(V_2^* - 2A_{22}) \quad (\text{B.15})$$

And solving for $A_{21} - A_{22}$ one finds:

$$A_{21} - A_{22} = \frac{V_1^*(1 + \chi)}{2} - \frac{V_2^*(1 + \frac{1}{\chi})}{2} \quad (\text{B.16})$$

For a latch in the ideal metastable state, $A_{21} = A_{22}$, or

$$V_1(0) = \frac{V_2(0)}{\chi} \quad (\text{B.17})$$

Notice that in this case, it also individually results $A_{21} = 0, A_{22} = 0$, so that the growing modes are not only equal but completely suppressed. Assuming $V_1^* + V_2^* = 2V_{cm}$, $V_1 = \frac{\chi}{\chi+1}V_{cm}, V_2 = \frac{1}{\chi+1}V_{cm}, V_1^* - V_2^* = \frac{\chi-1}{\chi+1}V_{cm}$ is found and finally, called A_v the tracking mode gain of the latch,

$$V_{io} = \frac{V_{cm}}{A_v} \frac{\chi - 1}{\chi + 1} \quad (\text{B.18})$$

, where the first term depends on tracking mode comparator design, while the second only depends on regeneration phase parameters. For the realistic assumption $C_1 = C, C_2 = C + \Delta C, G_1 = G_2$, then $\chi = \sqrt{1 + \frac{\Delta C}{C}}$ and by expanding into first-order Taylor series,

$$V_{io} = \frac{\Delta C}{2C} \frac{V_{cm}}{A_v}$$

is finally found. If for instance $C = 20fF, \Delta C = 1fF, V_{cm} = 400mV, A_v = 1$, $V_{io} = 40mV$ is obtained. To verify the model, the circuit in figure B.1 was simulated in SPECTRE. Setting $V_{cm} = 500mV, C = 1p, G_m = 1\mu S$, and ΔC

successively .1pF,.5pF,.01pF, offset voltages of 24mV,101mV and 2.5mV were found, which match values calculated through B.18 almost perfectly.

The situation depicted is however not realistic, as the equilibrium point of the latch is assumed to be ground. Including a non-zero equilibrium point V^* , the differential equations for the circuit become

$$C_1 \frac{dV_1}{dt} = -G_1(V_2 - V^*) \quad (\text{B.19})$$

$$C_2 \frac{dV_2}{dt} = -G_2(V_1 - V^*) \quad (\text{B.20})$$

The amplitudes of the growing modes can be in this case more readily evaluated by using Laplace transforms to obtain $V_1(s)$ and $V_2(s)$, and successively using the residue theorem. Called A_{31} the amplitude of the growing mode on node V_1 , and A_{32} the amplitude of the growing mode on node V_2 ,it results

$$A_{31} = \tau \frac{V^*(1 - \chi) - V_1^* + V_2^* \chi}{2} \quad (\text{B.21})$$

$$A_{32} = \tau \frac{V^*(1 - \frac{1}{\chi}) - V_2^* + V_1^* \frac{1}{\chi}}{2} \quad (\text{B.22})$$

Both modes are annihilated if $V_1^* = V^*(1 - \chi) + V_2^* \chi$. By substituing $V_1^* + V_2^* = 2V_{cm}$ and performing some algebra, the final equation results

$$V_{io} = \frac{2(V_{cm} - V^*)}{A_v} \frac{\chi - 1}{\chi + 1} \quad (\text{B.23})$$

Simulations performed on a modified latch model show perfect agreement with predictions. For instance, considering $V^* = 250mV, V_{cm} = 500mV, C = 50fF, \Delta C = (1f, 10f, 50f)$ the simulated offset was 2.45mV,32mV,80mV while the computed values are 2.5mV,32mV,85mV. We also compared such results with full circuit level simulations of the proposed comparator. The results are shown in figure B.2. The reason for the inaccuracy is the dependance of the comparator calibration LSB on non-overlap time, shown in figure B.3. In the limit of very small non-overlap times, the calculated and the calculated values agree. Because the non-overlap time seen by the comparator is larger than that used to size the calibration capacitors(See Tab. B.1, this might also be a rationale for the reduced effectiveness of the calibration routine.

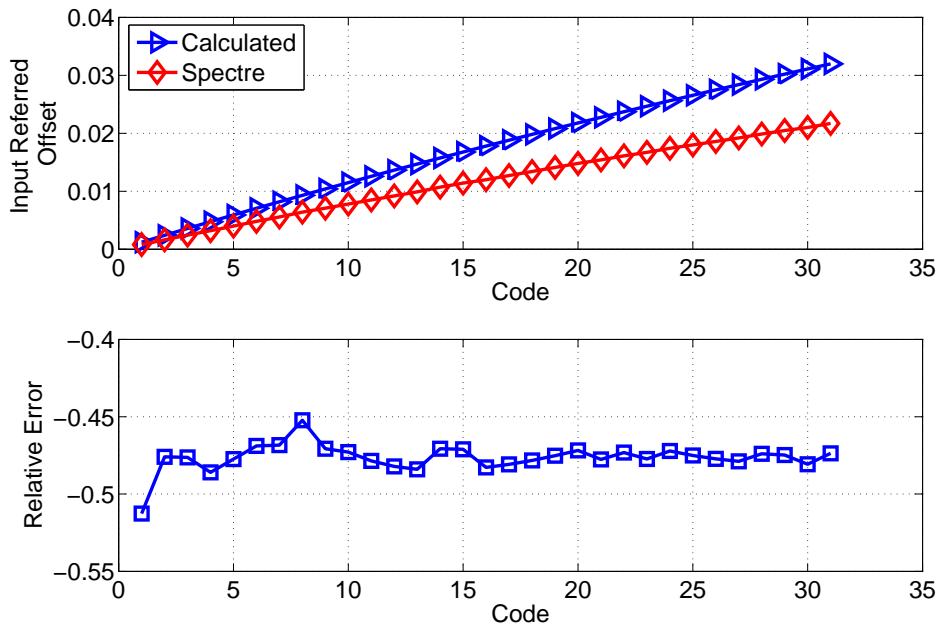


Figure B.2: Calculated and simulated offset values

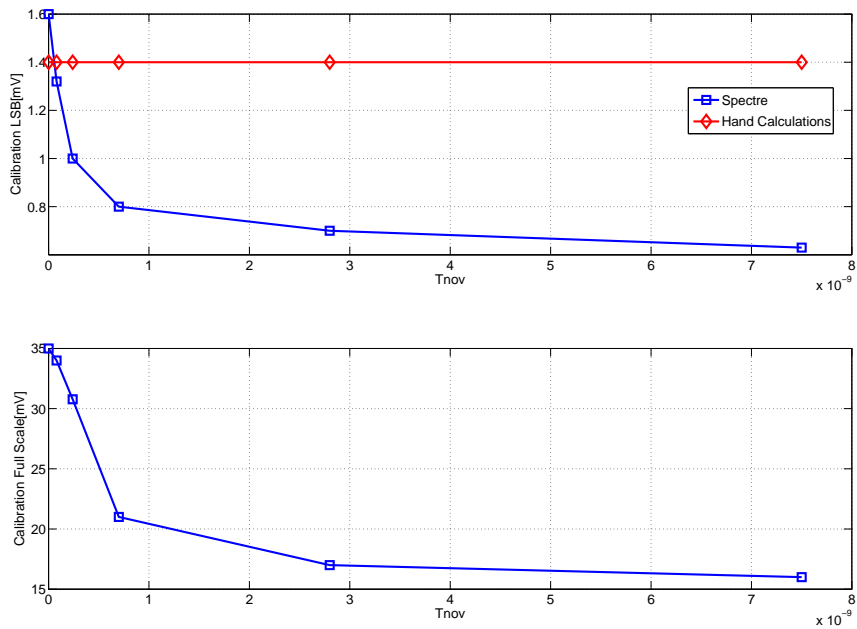


Figure B.3: Simulated offset value versus non-overlap time

Process Corner	FF	TT	SS
T_{nov}	1.8n	2.4n	3.3n

Table B.1: Simulated Embedded Comaprator Non-Overlap Time. The value of T_{nov} used for design of the calibration array was 1nS

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