CHUA'S CIRCUIT WITH CURRENT-OFFSET CHUA DIODE

by

Michael Peter Kennedy

Memorandum No. UCB/ERL M92/47

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Abstract

This circuit uses a current source to force a current offset in the piecewise-linear characteristic of a Chua diode. The modified Chua diode consists of a negative resistance converter, two ideal diodes, and a current source.

1 Circuit description

Arrays of Chua's circuits have been shown by simulation to exhibit interesting wave propagation effects [PMPVC92]. This work is motivated by the need for identical Chua's circuits each of which can be altered in a similar manner by a single control signal.

We define Chua's diode [Ken92b] as any two-terminal nonlinear resistor which is described by an *active* but eventually passive [Chu69] *v-i* characteristic. This class of active nonlinear resistors was first identified by Leon Chua in the 1960s as the fundamental building blocks for nonlinear oscillation. Since then, he has developed comprehensive synthesis procedures for these elements [Chu69].

The *v-i* characteristic of a voltage-controlled nonlinear resistor may be offset along the *i*-axis by adding a current source in parallel with the element [CDK87]. This is illustrated in Figs. 1 and 2.

Chua's circuit using a current-offset Chua diode is shown in Fig. 3.

The desired nonlinear resistor characteristic is obtained by connecting in parallel a negative impedance converter (N_{R1}), two ideal diodes (N_{R2} and N_{R3}) [Ken92a], and a Howland current source (N_{R4}) [Ana92].

A negative resistance converter N_{R1} (A_1, R_1, R_2, and R_3) is used to produce the underlying negative resistance. Connected in parallel with the negative impedance converter are two ideal diodes [CDK87] (A_2, R_4, D_1) and (A_3, R_8, D_2) with dc offsets set by V^+, R_5, and R_6, and V^-, R_9, and R_{10} respectively. These connect a positive resistance R_7 in parallel with the negative resistor N_{R1} whenever the voltage v_R exceeds the breakpoints BP^- and BP^+ in magnitude. N_{R4} supplies the desired dc offset current I_{OS}.

This architecture allows one to control independently the slopes, breakpoints, and current offset of the Chua diode's *v-i* characteristic. In addition, several circuits may be adjusted simultaneously by applying the same voltage V_{OS} to each circuit.

2 Example

We consider the case $BP^+ = BP^- = 1\text{V}$, and $\alpha = 10$, $\beta = 39$.

Using a dual 15V supply to power the op amps gives $V^+ = 15\text{V}$ and $V^- = -15\text{V}$.

A complete list of components is given in Table 1. In addition, the power supplies should be decoupled by connecting two 100 nF capacitors from pins 4 and 11 of the 14-pin quad op amp package to ground as close to the package as possible.

- Resistor pairs R_5, R_6 and R_9, R_{10} act as voltage dividers to set the breakpoints of the *v–i* characteristic at

$$-BP^- = -\frac{1.00}{1.00+14.0}15\text{V} = -1\text{V}, \qquad BP^+ = \frac{1.00}{1.00+14.0}15\text{V} = 1\text{V}$$

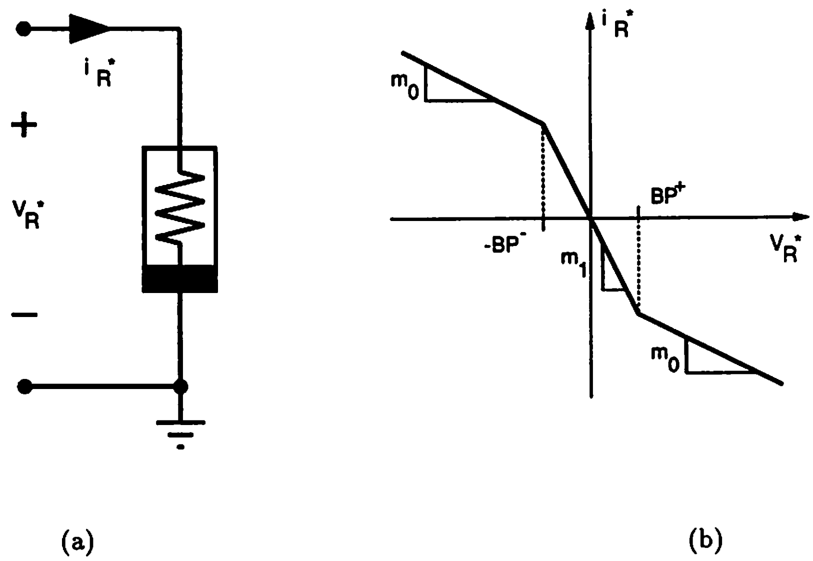


Figure 1: Chua diode (a) and its v-i characteristic (b).

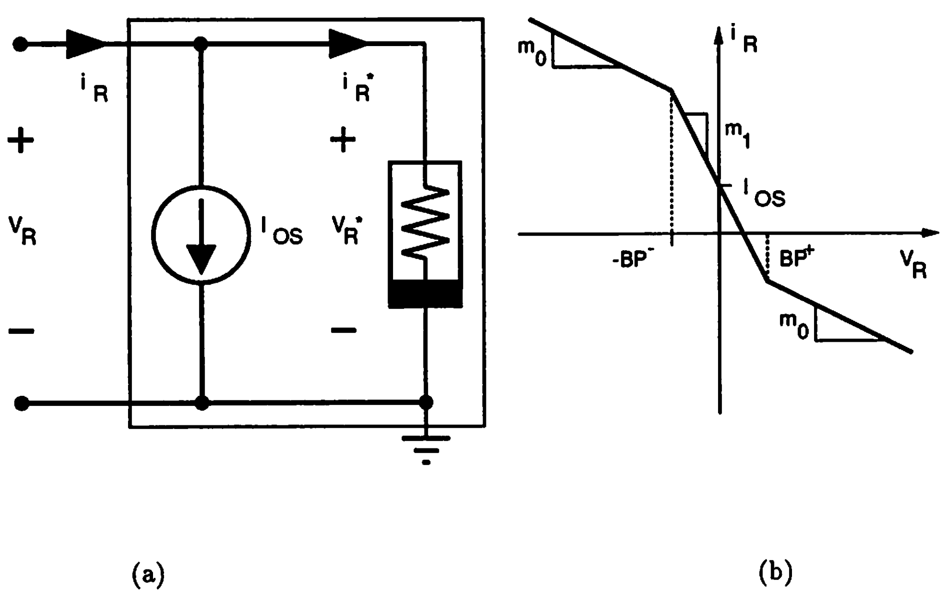


Figure 2: (a) A current source I_{OS} in parallel with the nonlinear resistor produces a current offset in the v-i characteristic (b).

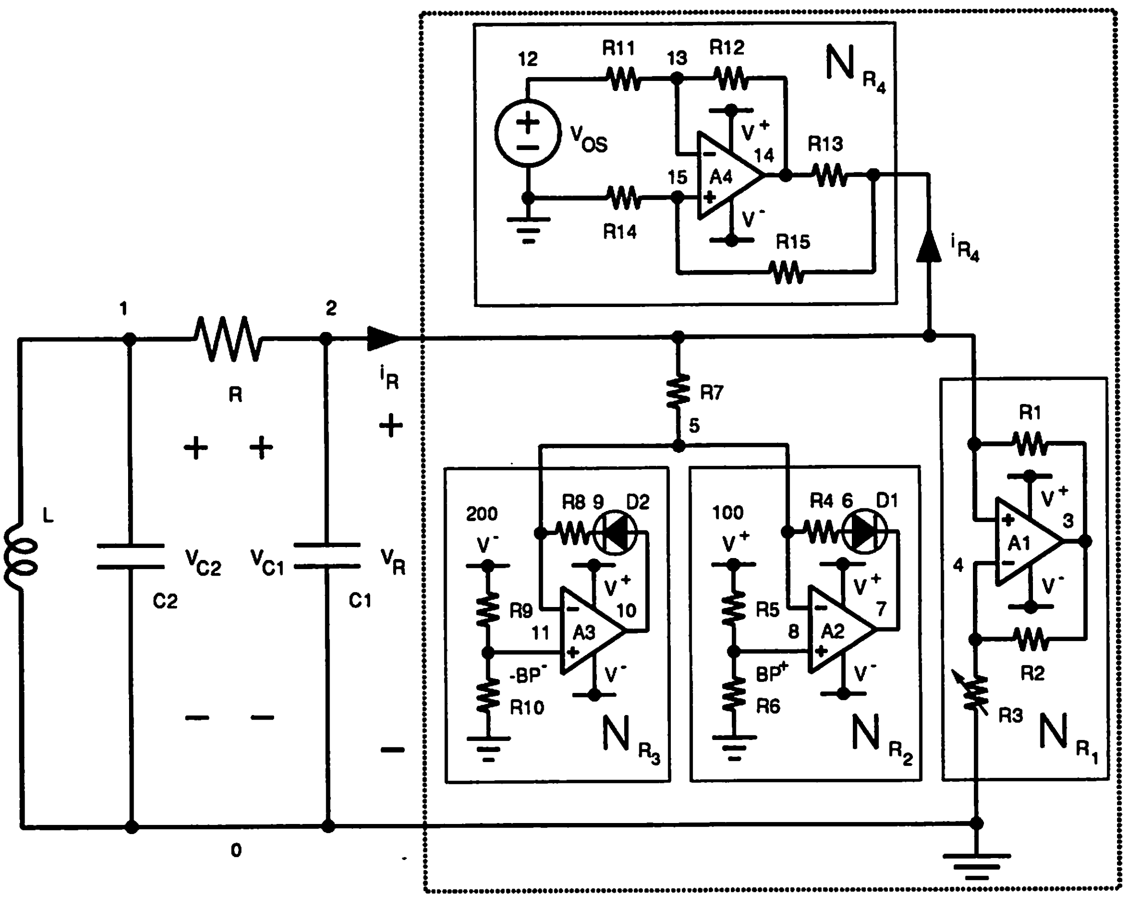


Figure 3: Realization of Chua's circuit using a current-offset Chua diode. The basic nonlinear resistor is constructed by connecting a negative resistance converter N_{R1} in parallel with two parallel-connected ideal diodes with dc offsets (N_{R1} and N_{R2}) in series with a linear resistor R_7. The offset current is provided by a current source N_{R4}.

Element	Description	Value	Tolerance
N_{R_1}	Negative resistance converter		
A_1	$\frac{1}{4}$ AD713K quad BiFET op amp		
R_1	$\frac{1}{4}$W Resistor	150 Ω	±1%
R_2	$\frac{1}{4}$W Resistor	150 Ω	±1%
R_3	20-turn cermet trimmer	1.00 kΩ	±1%
R_7	$\frac{1}{4}$W Resistor	2.32 kΩ	±1%
N_{R_2}	Series ideal diode and voltage source		
A_2	$\frac{1}{4}$ AD713K quad BiFET op amp		
D_1	1N4148 silicon switching diode		
R_4	$\frac{1}{4}$W Resistor	2.20 kΩ	±5%
R_5	$\frac{1}{4}$W Resistor	14.0 kΩ	±1%
R_6	$\frac{1}{4}$W Resistor	1.00 kΩ	±1%
N_{R_3}	Series ideal diode and voltage source		
A_3	$\frac{1}{4}$ AD713K quad BiFET op amp		
D_2	1N4148 silicon switching diode		
R_8	$\frac{1}{4}$W Resistor	2.20 kΩ	±5%
R_9	$\frac{1}{4}$W Resistor	14.0 kΩ	±1%
R_{10}	$\frac{1}{4}$W Resistor	1.0 kΩ	±1%
N_{R_4}	Current source		
A_4	$\frac{1}{4}$ AD713K quad BiFET op amp		
R_{11}	$\frac{1}{4}$W Resistor	1.00 MΩ	±1%
R_{12}	$\frac{1}{4}$W Resistor	2.00 kΩ	±1%
R_{13}	$\frac{1}{4}$W Resistor	100 Ω	±1%
R_{14}	$\frac{1}{4}$W Resistor	1.00 MΩ	±1%
R_{15}	$\frac{1}{4}$W Resistor	2.00 kΩ	±1%
C_1	Capacitor	39 nF	±2%
R	$\frac{1}{4}$W Resistor	1.00 kΩ	±1%
C_2	Capacitor	390 nF	±2%
L	TOKO type 10RB fixed inductor	10 mH	±10%

Table 1: Complete component list for Chua's circuit with current offset in the Chua diode characteristic.

- The slope of the v-i characteristic over its central region (for the special case $R_1 = R_2$ and $R_{11}/R_{12} = R_{14}/R_{15}$) is given by

$$m_1 \approx -\frac{R}{R_3} + \frac{R}{R_{11} + R_{12}},$$

where $R_{11} + R_{12}$ is the approximate output impedance of the current source in its linear region. With $R = 1.00$ kΩ, $R_{11} = 1.00$ MΩ and $R_{12} = 2.00$ kΩ, a desired value of -8/7 for m_1 forces us to choose

$$R_3 \approx 874\Omega.$$

Set R_3 to 874 Ω by adjusting the 1 kΩ cermet trimmer.

- The slope m_0 outside the breakpoints is determined from

$$m_0 = m_1 + \frac{R}{R_7}$$

Selecting $m_0 = -5/7$ gives

$$R_7 = 2.333\text{k}\Omega.$$

We use the standard value 2.32 kΩ instead.

- With $R_{11}/R_{12} = R_{14}/R_{15}$, the current offset is given by

$$I_{OS} = \frac{R_{12}}{R_{11}R_{13}} V_{OS}.$$

For this set of resistor values,

$$I_{OS} = 0.02 V_{OS} \text{ mA},$$

where V_{OS} is measured in Volts. For example, $V_{OS} = 5$ V gives an offset of $I_{OS} = 0.1$ mA. Over the linear region of A_4,

$$i_{R4} \approx I_{OS}$$

- The normalized circuit parameters are given by:

$$\begin{aligned} \alpha &= \frac{C_2}{C_1} \\ &= 10 \end{aligned}$$

and

$$\begin{aligned} \beta &= \frac{C_2 R^2}{L} \\ &= 39. \end{aligned}$$

3 SPICE simulation

The SPICE deck in Fig. 4 may be used to simulate the behavior of the current-offset Chua's circuit. The AD713 op amp [Ana90] is modeled by Analog Devices' AD713 SPICE macro-model [Ana91]. Node numbers are as in Fig. 3. The power rails are 100 and 200.

The v-i characteristic may be verified by means of the SPICE deck shown in Fig. 5. The characteristics for $V_{OS} = 0$ V and $V_{OS} = 10$ V are shown in Figs. 6(a) and (b) respectively.

Acknowledgements

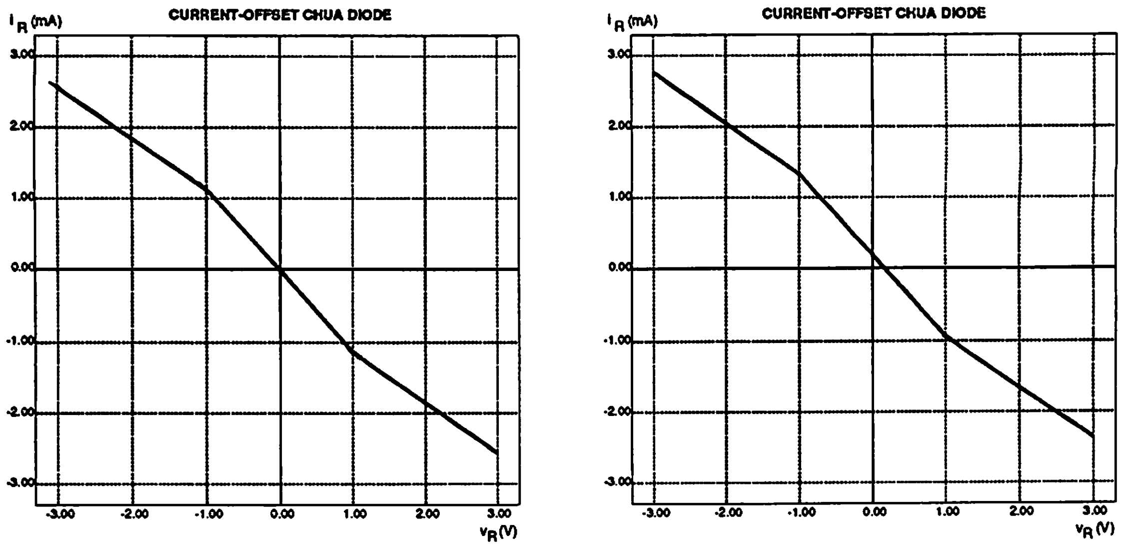
This work is supported in part by the National Science Foundation under Grant MIP 89-12639 and by the Office of Naval Research under Grant N00014-89-J-1402. Thanks to Vicente Perez-Munuzuri who prompted me to design this circuit and to Kevin Eckert who verified it experimentally.

```
CHUA'S CIRCUIT WITH CURRENT-OFFSET CHUA DIODE

V+ 100 0   DC 15
V- 0  200  DC 15

XA1  2 4 100 200 3 AD713
R1   2 3  150
R2   3 4  150
R3   4 0  874

XA2  8 5 100 200 7 AD713
R4   5 6  2200
D1   6 7  D
R5   100 8  14k
R6   8 0   1k

R7   2 5  2320

XA3  11 5 100 200 10 AD713
R8   5 9  2200
D2   10 9 D
R9   200 11  14k
R10  11 0   1k

VOS  12 0   DC 10
XA4  15 13 100 200 14 AD713
R11  12 13   1000k
R12  13 14   2k
R13  14 2    100
R14  0  15   1000k
R15  15 2    2k

* AD713 SPICE Macro-model      1/91, Rev. A
*
* This version of the AD713 model simulates
* the typical parameters corresponding to
* those in the data book.
*
* Copyright 1991 by Analog Devices, Inc.
*
* connections: non-inverting input
*              — inverting input
*              — — positive supply
*              — — — negative supply
*              — — — — output
*              — — — — —
.SUBCKT AD712 13 15 12 16 14
*
VOS 15 8 DC 0
EC 9 0 14 0 1
C1 6 7 .5P
RP 16 12 12K
GB 11 0 3 0 1.67K
RD1 6 16 16K
RD2 7 16 16K
ISS 12 1 DC 100U
CCI 3 11 150P
GCM 0 3  0 1  1.76N
GA 3 0  7 6  2.3M
RE 1 0 2.5MEG
RGM 3 0 1.69K
VC 12 2 DC 2.8
VE 10 16 DC 2.8
RO1 11 14 25
CE 1 0 2P
RO2 0 11 30
RS1 1 4 5.77K
RS2 1 5 5.77K
J1 6 13 4 FET
J2 7 8 5 FET
DC 14 2 DIODE
DE 10 14 DIODE
DP 16 12 DIODE
D1 9 11 DIODE
D2 11 9 DIODE
IOS 15 13 5E-12
.MODEL DIODE D
.MODEL FET PJF(VTO=-1 BETA=1M IS=25E-12)
.ENDS

C1 2 0 39n
R  1 2 1k
C2 1 0 390n
L  1 0 10m

.WIDTH OUT=80
.IC V(2)=0.1 V(1)=0.0
.TRAN 0.1ms 50ms
.PRINT TRAN V(2) V(1) I(VSENSE)
.PLOT TRAN V(2) V(1) I(VSENSE)
.END
```

Figure 4: SPICE deck to simulate the transient response of Chua's circuit with current-offset Chua diode. Node numbers are as in Fig. 3. The op amps are modeled by the AD713 macro-model from Analog Devices.

```
CHUA'S CIRCUIT WITH CURRENT-OFFSET CHUA DIODE

V+  100 0    DC 15
V-  0   200  DC 15

XA1  2 4 100 200 3 AD713
R1   2 3  150
R2   3 4  150
R3   4 0  874

XA2  8 5 100 200 7 AD713
R4   5 6  2200
D1   6 7  D
R5   100 8  14k
R6   8 0    1k

R7   2 5  2320

XA3  11 5 100 200 10 AD713
R8   5 9  2200
D2   10 9 D
R9   200 11  14k
R10  11 0    1k

VOS  12 0    DC 10
XA4  15 13 100 200 14 AD713
R11  12 13   1000k
R12  13 14   2k
R13  14 2    100
R14  0  15   1000k
R15  15 2    2k

* AD713 SPICE Macro-model       1/91, Rev. A
*
* This version of the AD713 model simulates
* the typical parameters corresponding to
* those in the data book.
*
* Copyright 1991 by Analog Devices, Inc.
*
* connections: non-inverting input
*              — inverting input
*              — — positive supply
*              — — — negative supply
*              — — — — output
*              — — — — —
.SUBCKT AD712 13 15 12 16 14
*
VOS 15 8 DC 0
EC 9 0 14 0 1
C1 6 7 .5P
RP 16 12 12K
GB 11 0 3 0 1.67K
RD1 6 16 16K
RD2 7 16 16K
ISS 12 1 DC 100U
CCI 3 11 150P
GCM 0 3  0 1  1.76N
GA 3 0  7 6  2.3M
RE 1 0 2.5MEG
RGM 3 0 1.69K
VC 12 2 DC 2.8
VE 10 16 DC 2.8
RO1 11 14 25
CE 1 0 2P
RO2 0 11 30
RS1 1 4 5.77K
RS2 1 5 5.77K
J1 6 13 4 FET
J2 7 8 5 FET
DC 14 2 DIODE
DE 10 14 DIODE
DP 16 12 DIODE
D1 9 11 DIODE
D2 11 9 DIODE
IOS 15 13 5E-12
.MODEL DIODE D
.MODEL FET PJF(VTO=-1 BETA=1M IS=25E-12)
.ENDS

VSENSE 1 2 DC 0

VIN 1 0 PWL(0.0 0.0  0.25 3.0  0.75 -3.0  1.0 0.0)

.WIDTH OUT=80
.IC V(2)=0.1  V(1)=0
.TRAN 1.0MS 1.0S
.PRINT TRAN V(2) V(1) I(VSENSE)
.PLOT TRAN V(2) V(1) I(VSENSE)
.END
```

Figure 5: SPICE deck to plot the v-i characteristic of the current-offset Chua diode in Fig. 3. As before, the op amps are modeled by the AD713 macro-model from Analog Devices.



(a) (b)

Figure 6: Simulated *v-i* characteristic of current-offset Chua diode on the right of Fig. 3. (a) $V_{OS} = 0$ V — no offset; (b) $V_{OS} = 10$ V — 0.2 mA offset.

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