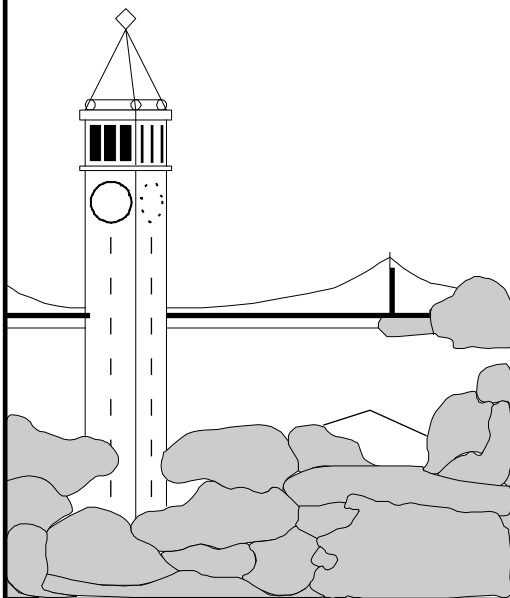


Cache Performance for Multimedia Applications

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Abstract

The caching behavior of multimedia applications has been described as having high instruction reference locality within small loops, very large working sets, and poor data cache performance due to non-locality of data references. Despite this, there is no published research deriving or measuring these qualities. Utilizing the previously developed Berkeley Multimedia Workload, we present the results of execution driven cache simulations with the goal of aiding future media processing architecture design. Our analysis examines the differences between multimedia and traditional applications in cache behavior. We find that multimedia applications actually exhibit lower instruction miss ratios and comparable data miss ratios when contrasted with other widely studied workloads. In addition, we find that longer data cache line sizes than are currently used would benefit multimedia processing.

1 Introduction

Multimedia is an amalgamation of various data types such as audio, 2D and 3D graphics, animation, images and video within a computing system or within a user application [Bhas97]. Put simply, a *multimedia application* is one which operates on data to be presented visually or aurally. The purpose of this work is to explore the cache behavior of real world multimedia applications. An important motivation is the widespread belief (seemingly without any actual basis in research) that data caches are not useful for multimedia applications because of the streaming nature of the data upon which they operate [Cont97], [Dief97], [Kuro98], [Lee96], [Rixn98]. The results presented in this paper strongly suggest that contemporary media processing applications perform no worse than traditional integer and floating point workloads.

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2 Related Work

There have been a limited number of multimedia caching studies. [Sode97] studied the data cache behavior of MPEG-2 video decoding with the goal of optimizing playback performance through the cache sensitive handling of the data types used. It was found that although it has been suggested that caches are critically inefficient for video data (several media processor chips dispense with data caches entirely), there was sufficient reuse of values for caching to significantly reduce the raw required memory bandwidth. [Haku97], [Cox98], [Vart98] have studied the usefulness of caching the textures used in 3D rendering. A texture cache with a capacity as small as 16 KB has been found to reduce the required memory bandwidth three to fifteen times over a non-cached design and exhibit miss ratios around 1% [Haku97]. The addition of a larger second level of texture cache (2 MB) to a small first level cache (2 KB) can reduce the memory bandwidth from 475 MB/s to around 92 MB/s [Cox98].

There have been several studies of prefetching for multimedia. [Zuck96] examined several hardware data prefetching techniques for MPEG-1 (encoding and decoding) and MPEG-2 (decoding). Three hardware prefetching techniques were considered, with the most successful found to reduce the miss count by 70% to 90%. [Stru98] presents a combined hardware/software solution to prefetching for multimedia. Based on cycle accurate simulation of the Trimedia VLIW processor running a highly optimized video de-interlacing application, it was found that such a prefetching scheme was able to eliminate most data cache misses, with the effectiveness dependent on the timing parameters involved. [Cucc99] suggests a two-dimensional prefetching strategy for image data, due to the two separate degrees of spatial locality inherent in image processing (horizontal and vertical). When their 2D prefetching technique was applied to MPEG-2 decoding as well as two imaging applications (convolution and edge tracing), 2D prefetch was found to reduce the miss ratio more than one block look-ahead. Hardware implementation aspects of prefetching are discussed in [Tse98].

3 Multimedia Workload

3.1 Description

For our study of the cache behavior of multimedia applications, we employ the Berkeley Multimedia Workload, which we develop and characterize in [Sling00a]. A description of the component applications and data sets is given in Table 1. The main driving force behind application selection was to strive for completeness in covering as many types of media processing as possible. Open source software was used both for its portability (allowing for cross platform comparisons) as well as the fact that we could directly examine the source code.

The Berkeley workload represents the domains of *3D graphics* (Doom, Mesa, POVray), *document and image rendering* (Ghostscript, DjVu, JPEG), *broadband audio* (ADPCM, LAME, mpg123, Timidity), *speech* (Rsynth, GSM, Rasta) and *video* (MPEG-2). Three MPEG-2 data sets are included to cover Digital Video Disc (DVD) and High Definition Television or HDTV (720P, 1080I) resolutions. The parameters of the DVD, and HDTV data sets are listed in the table below:

Format	Aspect	Horizontal	Vertical	Frames
DVD	4:3	720	480	16
HDTV 720P	16:9	1280	720	16
HDTV 1080I	16:9	1920	1080	16

All of the applications in the Berkeley Multimedia Workload are written in C with the exception of DjVu which is coded in C++. Data sets were chosen to be on the order of real workloads, with long enough traces (instruction and data) to exercise very large caches. The trace lengths and other relevant simulation characteristics are listed in Table 2. Total simulation time for our work, not including false starts, machine down time and other simulation problems, was 24.4 days of CPU time for each multimedia run, once with and once without multiprogramming, and 147.2 days of CPU time for SPEC95 simulations, for a grand total of 196 days of CPU time. The machine used was a DEC AlphaStation 255 workstation with a 300 MHz Alpha 21064a).

As it is often necessary to reduce large values of simulation results into a more easily digestible form, we will use averaging where necessary to compress results. Because the number of applications representing a particular application domain (audio, speech, document, video, 3D) is arbitrary, we will let each of the five application domains comprise a total of 20% of the averaged workload result, with the component applications of each domain being weighted equally.

3.2 Motivation

Motivating our detailed study of the cache behavior of multimedia applications is the large role memory latency plays in limiting performance. The memory hierarchy parameters of bandwidth and latency were measured for several current systems and are shown in Table 3 (the methodology used to obtain these parameters is detailed in the Appendix). Consider Table 4, which compares performance with caching against

the same system with all cache levels (L1 and L2) disabled. This was done by setting the appropriate BIOS parameters on our test system at boot time and then measuring the performance on real hardware. From this experiment we can see that modern microprocessor performance is highly dependent on an efficient memory hierarchy. The difference in latency between different levels of contemporary memory hierarchies is substantial, explaining the enormous slowdown we observed when the cache was disabled on our test system. Note that the system time (time spent in the operating system) slowdown is considerably less than that of the user time. This corroborates the generally held belief that the memory locality within operating system code is very poor, as it exhibits less of a performance degradation when caching is disabled.

Name	User Time Ratio	Sys Time Ratio
ADPCM Encode	25.0	3.6
ADPCM Decode	32.9	11.3
DJVVU Encode	56.7	3.6
DJVVU Decode	61.0	16.8
Doom	53.0	1.4
Ghostscript	63.7	34.7
GSM Encode	61.3	6.7
GSM Decode	77.8	16.5
JPEG Encode	103.4	1.3
JPEG Decode	103.0	10.5
LAME	80.3	1.4
Mesa Gears	44.2	11.0
Mesa Morph3D	35.9	35.0
Mesa Reflect	77.4	17.5
MPEG-2 Encode DVD	86.3	2.3
MPEG-2 Encode 720P	82.9	1.4
MPEG-2 Encode 1080I	86.5	1.5
MPEG-2 Decode DVD	94.1	9.3
MPEG-2 Decode 720P	95.1	5.9
MPEG-2 Decode 1080I	91.9	10.4
mpg123	83.7	7.5
POVray3	74.5	16.0
Rasta	83.8	7.0
Rsynth	86.5	27.0
Timidity	73.9	20.3
Arithmetic Mean	72.6	11.2
Geometric Mean	68.6	7.1

Table 4: **Uncached Performance Slowdown Factor** - ($t_{uncached}/t_{cached}$) when L1 and L2 caches were disabled on a 500 MHz AMD Athlon, 64 Kbyte L1 data cache, 64 Kbyte L1 instruction cache, 512 Kbyte L2 unified cache, 64-byte line size.

As another way to see the importance that caches play in modern computer performance, the actual measured total user time for each application was compared with the optimal user run time (a computed result based on the number and type of instructions executed) reported by the DEC ATOM pixie tool, which does not include memory latency and other effects in its measurements. Thus, the pixie results represent

Name	Description	Data Set
ADPCM	IMA ADPCM audio compression	Excerpt from Shchedrin’s Carmen Suite, 28 sec., Mono, 16-bits, 44 kHz
DjVu	AT&T IW44 wavelet image compression	491x726 color digital photographic image
Doom	Classic first person shooter video game	25.8 sec. recorded game sequence (774 frames @ 30 fps)
Ghostscript	Postscript document viewing/rendering	First page of Rosenblum and Ousterhout’s LFS paper (24.8 KB)
GSM	European GSM 06.10 speech compression	Speech by U.S. Vice President Gore, 24 sec., Mono, 16-bits, 8 kHz
JPEG	DCT based lossy image compression	491x726 color digital photographic image
LAME	MPEG-1 Layer III (MP3) audio encoder	Excerpt from Shchedrin’s Carmen Suite, 28 sec., Stereo, 16-bits, 44 kHz
Mesa	OpenGL 3D rendering API clone	Animated gears, morph3d, reflect demos - 30 frames each at 1024x768
MPEG-2	MPEG-2 video encoding	16 frames (1 GOP) at DVD, HDTV 720P, HDTV 1080I resolutions
mpg123	MPEG-1 Layer III (MP3) audio decoder	Excerpt from Shchedrin’s Carmen Suite, 28 sec., Stereo, 16-bits, 44 kHz
POVray	Persistence of Vision ray tracer	640x480 Ammonite scene by artist Robert A. Mickelson
Rasta	Speech recognition	2.128 sec. SPHERE audio file: “Laurie?...Yeah...Oh.”
Rsynth	Klatt speech synthesizer	181 word excerpt of U.S. Declaration of Independence (90 sec., 1,062 bytes)
Timidity	MIDI music rendering with GUS instruments	X-files theme song, MIDI file (49 sec., 13,894 bytes), Goemon patch kit

Table 1: Berkeley Multimedia Workload

the best possible execution time for a given sequence of instructions. We assume that memory latency is the dominant factor for why measured performance does not match the theoretically optimal performance. The comparison is shown for DEC AlphaStation 255 workstations with a 300 MHz Alpha 21064a processor and 128 MB of RAM in Table 5.

4 Methodology

In order to measure cache miss ratios, we modified the LibCheetah v2.1 implementation [Aust] of the trace driven Cheetah cache simulator [Sugu93] to operate in an execution driven mode. It was also extended to allow for traces longer than 2^{31} references long. Cheetah simultaneously evaluates many alternative uniprocessor caches, but restricts the design options that can be varied. For each pass through an address trace, all of the caches evaluated must have the same block size, do no prefetching, and use the LRU or MIN replacement algorithms. Other cache simulators were also considered for this study (TychoII [WARTS], Dinero IV [Edler]), but were found to be considerably slower than Cheetah or otherwise unsuitable for use in execution driven simulation due to dynamic memory allocation issues. (See [Uhl97] and [Smit94] for overviews of trace driven simulation in general, and [Roth99b] for a comparison of the performance of a variety of execution and trace driven solutions.) DEC’s ATOM [DEC] was used to instrument target applications with the modified Cheetah simulator, allowing for execution driven cache simulation.

4.1 Trace Length

Many cache studies utilize trace lengths that are a fraction of an application’s total run time due the enormous simulation times required to account for every instruction and data cache reference. Unfortunately, short trace lengths are problematic because programs exhibit phase behavior; an effect which is easily seen in Figure 1.

Name	Measured (sec)	Optimal (sec)	Percent Difference
ADPCM Encode	0.324	0.260	19.85%
ADPCM Decode	0.225	0.162	27.82%
DJVU Encode	2.482	1.592	35.86%
DJVU Decode	1.848	1.164	37.01%
Doom	9.150	7.605	16.89%
Ghostscript	6.370	3.454	45.78%
GSM Encode	2.511	2.375	5.42%
GSM Decode	0.739	0.717	2.98%
JPEG Encode	1.046	0.873	16.56%
JPEG Decode	0.537	0.433	19.33%
LAME	71.300	40.680	42.95%
Mesa Gears	3.450	1.152	66.61%
Mesa Morph3D	2.950	0.998	66.18%
Mesa Reflect	17.660	13.970	20.89%
MPEG-2 Encode DVD	74.428	64.630	13.16%
MPEG-2 Encode 720P	201.663	172.500	14.46%
MPEG-2 Encode 1080I	460.429	397.700	13.62%
MPEG-2 Decode DVD	5.760	4.971	13.70%
MPEG-2 Decode 720P	17.980	15.280	15.02%
MPEG-2 Decode 1080I	36.230	30.360	16.20%
mpg123	3.830	2.620	31.59%
POVray3	66.442	32.780	50.66%
Rasta	0.183	0.112	39.02%
Rsynth	2.282	2.005	12.14%
Timidity	35.223	32.150	8.72%
Arithmetic Mean			26.10%
Geometric Mean			20.55%

Table 5: Effect of Memory Latency on Execution Time - DEC AlphaStation 255 with 300 MHz Alpha 21064a processor, 16 Kbyte L1 instruction cache, 16 Kbyte L1 data cache, 1 Mbyte L2 unified cache

The graphs depict the number of cache misses per 1,000,000 instructions executed for two sample applications. A second

Name	Instruction References	Load References	Store References	Cache Purge Interval	Data Time	User Time	System Time	Max Resident Set Size (kB)
ADPCM Enc.	64,020,339	4,302,782	616,116	708,037	27.818	0.102	0.036	1,472
ADPCM Dec.	49,687,192	4,302,782	1,229,491	708,037	27.818	0.054	0.067	1,472
DJVVU Enc.	394,242,073	68,204,647	27,458,767	4,754,521	-	0.700	0.033	41,664
DJVVU Dec.	328,761,829	59,700,283	31,845,270	4,754,521	-	0.484	0.037	20,992
Doom	1,889,897,116	500,225,773	109,222,846	4,284,671	25.800	2.216	0.939	26,432
Ghostscript*	970,395,449	188,116,952	96,837,718	1,227,194	-	1.190	0.164	32,192
GSM Enc.	375,971,389	55,009,077	14,010,892	297,641	24.341	0.468	0.016	1,024
GSM Dec.	126,489,950	10,711,683	3,812,483	297,641	24.341	0.209	0.014	1,024
JPEG Enc.	177,977,854	41,182,069	14,156,413	3,821,284	-	0.223	0.006	10,880
JPEG Dec.	80,176,365	16,419,065	4,585,079	3,821,284	-	0.093	0.024	10,880
LAME*	7,989,818,554	1,688,230,256	720,826,607	3,358,692	27.818	18.543	0.075	7,104
Mesa Gears*	296,287,705	36,839,087	38,449,257	2,173,610	1.000	0.484	0.039	50,240
Mesa Morph3D*	239,456,087	28,181,931	42,865,365	2,173,610	1.000	0.467	0.050	50,432
Mesa Reflect*	2,752,665,912	431,196,702	221,523,544	2,173,610	1.000	3.672	0.051	59,968
MPEG2 Enc. DVD	17,986,999,069	3,257,725,765	554,222,287	5,339,432	0.533	17.896	0.199	48,128
MPEG2 Enc. 720P	47,606,551,352	8,581,717,942	1,563,082,541	5,339,432	0.533	48.263	0.505	124,032
MPEG2 Enc. 1080I	111,041,463,652	20,148,301,625	3,349,482,784	5,339,432	0.533	113.050	0.521	277,952
MPEG2 Dec. DVD	1,307,000,398	219,595,775	76,688,056	1,055,372	0.533	1.911	0.051	16,512
MPEG2 Dec. 720P	3,992,213,571	673,343,544	243,881,680	1,055,372	0.533	5.796	0.141	41,472
MPEG2 Dec. 1080I	8,038,214,930	1,341,912,185	464,649,094	1,055,372	0.533	12.098	0.182	91,648
mpg123*	574,034,774	166,675,525	45,334,678	1,554,505	27.818	0.735	0.015	3,328
POVray3	6,017,197,975	1,562,189,592	683,690,648	5,928,433	0.033	11.296	0.121	16,000
Rasta*	25,120,492	5,925,648	1,989,604	2,560,537	2.128	0.039	0.014	5,632
Rsynth	402,500,964	102,351,142	39,223,906	594,438	99.680	0.780	0.004	7,808
Timidity	4,588,632,916	1,340,471,112	594,047,710	3,675,086	47.440	2.036	0.104	25,664
Total	217,315,777,907	40,532,832,944	8,943,732,836	-	-	242.805	3.406	-
Arithmetic Mean	8,692,631,116	1,621,313,318	357,749,313	-	-	9.712	0.136	-

Table 2: **Berkeley Multimedia Workload Simulation Characteristics** - *data time* (inherent time represented in data set - machine independent), *user time* (time spent processing in user space - machine dependent), and *system time* (time spent processing in system space on behalf of an application - machine dependent) in seconds. The *cache purge interval* is the number of instructions executed in each context interval before flushing the simulated cache. *Resident Set* is the maximum number of kilobytes in memory active at any one time, as determined by the `getrusage()` system call. All measurements were done on a DEC Alpha DS20 workstation with dual 500 MHz Alpha 21264 processors and 2048 MB of RAM running Compaq Tru64 Unix v5.0A (Rev. 1094). All applications were compiled with GCC v2.8.1 except (*) compiled with DEC C v5.6-075.

System	L1 $t_{latency}$	L1 r_{xfer}	L2 $t_{latency}$	L2 r_{xfer}	Main Mem $t_{latency}$	Main Mem r_{xfer}
Microstar* AMD Athlon (500 MHz)	4.0 ns	2657.18 MB/s	109.7 ns	1182.90 MB/s	242.5 ns	305.76 MB/s
DEC DS10 Alpha 21264 (466 MHz)	4.3 ns	1939.14 MB/s	30.4 ns	825.27 MB/s	197.2 ns	336.92 MB/s
BX** Intel Pentium III (450 MHz)	4.4 ns	1695.97 MB/s	46.6 ns	806.94 MB/s	149.8 ns	308.33 MB/s
HP N-Class PA-8500 (3 x 450 MHz)	4.6 ns	2190.42 MB/s	-	-	293.3 ns	338.50 MB/s

Table 3: **Memory Latency and Bandwidth** - where $t_{latency}$ is the time delay for any memory transaction, consisting primarily of memory latency and address transmission time and r_{xfer} is the bus transfer rate or bandwidth in bytes transferred per unit time. (*)Microstar - Microstar 6167 motherboard utilizing AMD's AMD-750 chipset, Mandrake Linux v7.0, 256 MB RAM (**)BX - unknown motherboard employing the Intel 440BX chipset, RedHat Linux v6.0, 128 MB RAM

difficulty with short trace lengths specific to cache simulations is the *cold start* problem. Cache simulation programs typically start with an empty cache which becomes filled as the simulation progresses. All initial memory accesses will miss the cache (*compulsory* misses), so cold start effects can potentially dominate if traces are too short to mitigate these effects.

Traces of a billion or more references may be needed to fully initialize multi-megabyte cache configurations [Kess91].

In order to be able to simulate the effects of a program's behavior, it is necessary to have a trace which captures all of its behavior. We found that although there are some applications (notably many of the SPEC92/95 benchmarks) that exhibit

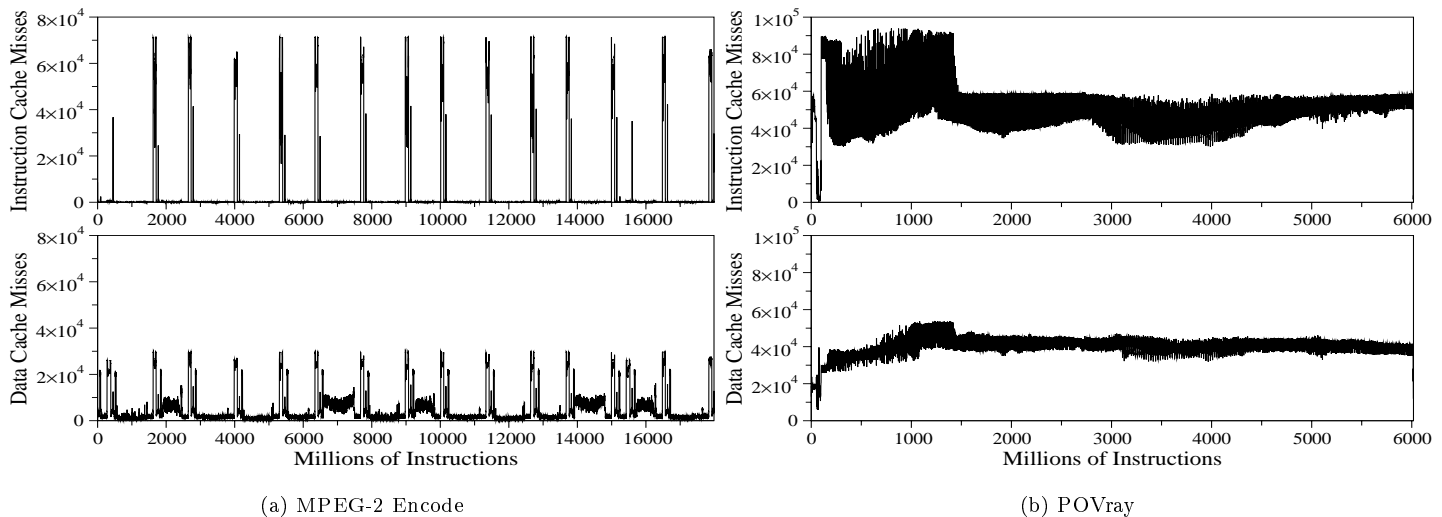


Figure 1: **Example Cache Miss Profiles** - the number of data cache misses per million instructions executed (direct mapped, 8Kbyte cache with 32 byte line size)

uniform cache behavior over their entire run times, our multimedia workload applications did not share this property. The result of this is that full applications traces are the only way to completely characterize cache behavior. Our work traces application programs with realistic data sets for full execution runs. The trace lengths for the component Berkeley Multimedia Workload applications are given in Table 2.

4.2 Operating System Behavior

In general, studies including operating system behavior are rare because of the difficulty involved in obtaining this information. User space is freely manipulated, but tracing system space usually requires that modifications be made to the operating system. Table 2 lists the amount of time the CPU spends either in user space (*user time*) doing actual work for the application, or in system space (*system time*) serving I/O requests and dealing with other overhead on behalf of the application. Both user time and system time are machine dependent, and vary based on the instruction set, clock cycle length and other architectural parameters. *Data time* is machine independent, and is the implicit time length of the data set. For example, 24 frames of DVD movie represent one second of data time, even though it may take only 0.5 seconds of actual computation time (the sum of system and user time) to process the data. Although our traces only include user state references, this represents almost all of the memory behavior of the programs under study; less than 1% of our multimedia workload was system time. To some degree this may be an artifact of the nature of the Berkeley Multimedia Workload, which involves only file I/O. In an actual multimedia application where data must be transferred to and from I/O devices such as network, disk, or sound and video controller cards, a larger amount of OS activity could be present.

4.3 Multiprogramming

Despite the fact that the Berkeley Multimedia Workload is dominated by user time computation, because of multiprogramming we cannot ignore operating system behavior. Although a quantum length that depends on clock time or external events remains constant with architectural change (10 to 100 ms), the number of cycles Q in each quantum has increased over time for various reasons, including less efficient software and a speedup of the processor relative to the speed of real time events. The number of cycles in a quantum affects cache miss ratio. When a context switch occurs, the instructions and data of the newly scheduled process may no longer be in the cache from the last time it was run due to the memory use of programs scheduled in the interim.

The effect of multiprogramming can be roughly approximated by periodically flushing (clearing) a simulated cache. In order to correctly simulate the effect of multiprogramming for our multimedia workload, the average context switching interval for commercial (closed source) Microsoft Windows applications was measured on real hardware. The applications were chosen to correspond as closely as possible to those comprising the Berkeley Multimedia Workload, such that, for example, the context interval measured for actual DVD video playback was used in our simulations of MPEG-2 video decoding at DVD resolutions. The context switch intervals of the actual applications from the Berkeley Multimedia Workload were not measured because they are primarily file based applications, typically converting between compressed and uncompressed format without presenting the resulting data to the user. So, although the algorithms they employ (and therefore their memory access patterns) should for the most part be realistically similar to their commercial counterparts, their scheduling behavior is vastly different. Microsoft Windows NT and Windows 2000 both maintain a large amount of performance information for a large number of system objects

including context switch count, user time and system time per thread. By dividing the sum of system time and user time by the measured context switch count it was possible to compute the average context switch interval for each type of application. The details of these measurements are given in the Appendix, with the simulation quanta (cache flush intervals) applied to each application listed in Table 2.

For comparison purposes, the SPEC95 benchmark suite was also simulated. SPEC95 was simulated without multiprogramming (cache flushing) for several reasons. First, it is normally run in a uniprogrammed mode in order to extract the highest benchmark performance [Gee93]. More importantly, when we measured the actual context switch intervals for SPEC95 on a modern DEC Alpha workstation (DS20 with dual 500 MHz Alpha 21264 processors), the context interval, Q , was measured to be sufficiently large such (2.2 million instructions, on average) that multiprogramming has very little effect on miss ratios (unlike multimedia applications which typically have several tightly cooperating threads, the SPEC applications are single threaded and entirely compute bound).

Many UNIX-type operating systems maintain context switch counts on a per process basis which is accessible through the `getrusage()` system call. The average context switch interval was computed in the same manner as for the Windows multimedia applications. The measured context switch intervals for SPEC95 are presented in the Appendix.

The component applications for both the multimedia workload and SPEC95 were compiled for the Alpha AXP architecture running Digital UNIX v4.0E with the default optimization levels in the case of the multimedia workload, and the base optimization level for SPEC95 (the same compiler optimization flags on all applications: `-fast -05 -non_shared`). The resulting binaries were then instrumented with the Cheetah cache simulator using ATOM and run on 300 MHz DEC Alpha AXP machines with 128 MB of RAM.

5 Simulation Results

The two major determinants of cache performance are *access time* (the latency from the beginning of an access until the time the requested data is retrieved) and *miss ratio* (the fraction of cache references which are not found in the cache) [Smit82]. Based on the latencies of a particular cache memory candidate design, in combination with the simulated or measured miss ratio, it is possible to select the design with the highest overall performance (lowest average memory access time) at some level of implementation cost.

Complete tables of the results from all of our simulations are available on the world wide web at <http://www.cs.berkeley.edu/~slingn/research/>, from which the cache performance of any application set of interest can be computed. For the sake of brevity, only overall average miss ratios are included in the Appendix.

5.1 Capacity

Capacity, or total cache size, has the greatest effect on miss ratio, and so it is one of the most important cache design parameters. Capacity, especially for L1 caches which are typically on the same die as the CPU, is limited by physical die size and implementation cost. In addition, the larger the capacity of a cache, the slower it is due to increased loading of critical address and data lines, thus requiring additional buffering [Przy88]. In order to study the effect of cache capacity on miss ratio, caches were simulated ranging in size from 1K to 2M bytes.

5.1.1 Other Workloads

The results of other studies, with a variety of workloads, on the effect of cache size on the miss ratio are presented alongside our simulation results for the Berkeley Multimedia Workload. All of the miss ratios presented in Figures 2, 3, and 4 are for caches with a line size of 32 bytes and two-way associativity, which represent common values for these parameters in current cache systems. Because the results shown have been gathered from a motley assortment of studies of disparate ages and architectures, many of which did not analyze configurations precisely identical to ours in terms of line size and associativity, we use adjusted results from [Gee93]. These adjustments modify the original results of the studies according to the ratios of miss ratios found in [Hill89] for differences in associativity, and [Smit87] for variations in line size. Extensions to larger cache sizes were made for the DTMR results using the $\sqrt{2}$ rule from [Smit82]. Each of the workloads is described in detail in the Appendix. It is important to note that many of the other studies included for comparison purposes also measured or simulated multiprogramming behavior, but because they are based on older machine architectures, their Q (quantum) lengths and therefore their context switch intervals are significantly shorter than those used in our simulations.

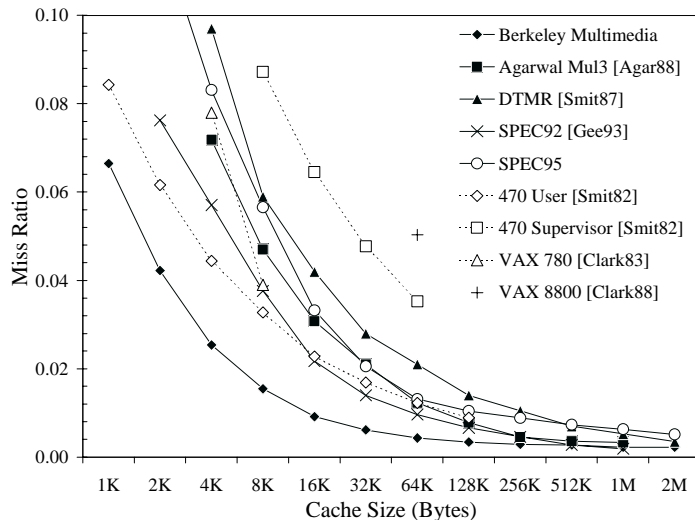


Figure 2: Unified Cache Miss Ratio - 32 byte line size

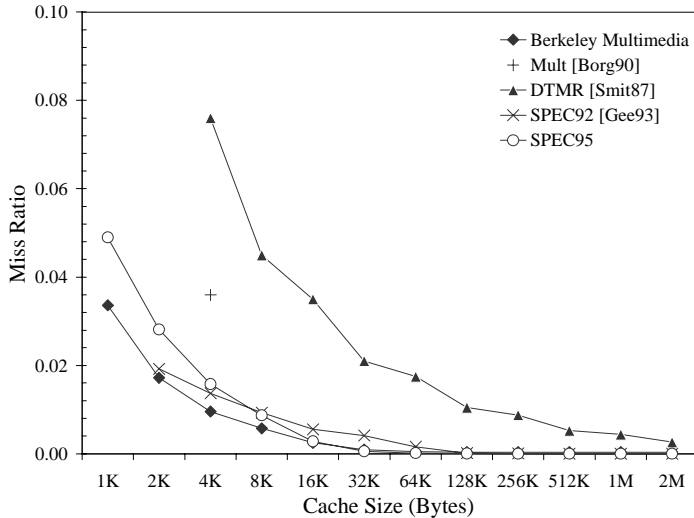


Figure 3: Instruction Cache Miss Ratio - 32 byte line size

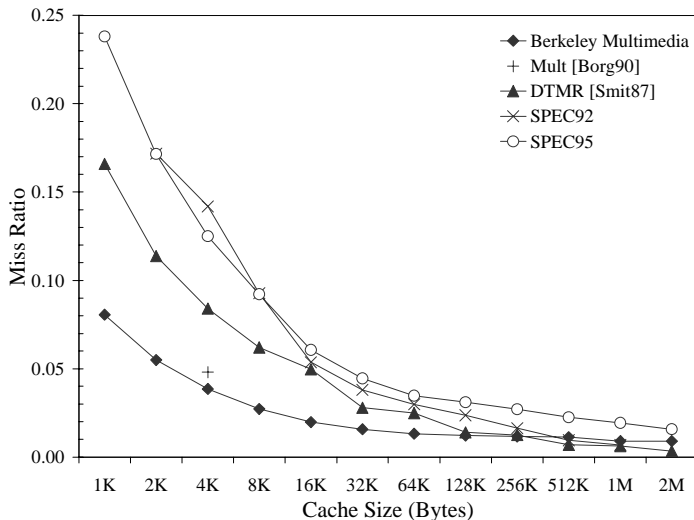


Figure 4: Data Cache Miss Ratio - 32 byte line size

The most significant result of Figures 2, 3, and 4 is that far from multimedia applications exhibiting degenerate cache behavior in comparison to more traditional workloads, our results demonstrate that they actually perform better for nearly all examined cache configurations. We believe that this is attributable to several factors. First, most of the comparison workloads are for timeshared machines on which task switching between users occurred very frequently. Further, the comparison studies are of architectures with much lower clock speeds than modern processors, and so exhibit higher miss ratios due to shorter context switch intervals based on real time periods. Even so, the uniprogrammed SPEC92 and SPEC95 benchmarks still demonstrate higher miss ratios than our multimedia workload. We believe that this is because many multimedia algorithm building blocks (such as the discrete cosine transform and fast Fourier transform) internally reference the same data locations repeatedly. In the case of

streaming multimedia applications, data is typically copied into a fixed region of memory (buffer) from the source file of network interface device. Even algorithms which simply traverse enormous arrays of data without re-referencing (color space conversion, subsampling) typically do so in linear memory order, and so benefit greatly from the “prefetching” effect of long cache lines. In addition, multimedia data types are typically small (8-bits for video and speech, 16-bits for audio, single precision (32-bit) floating point for 3D geometry calculations). This means that in comparison to the other workloads which utilize full 32-bit integers or 64-bit (double precision) floating point, more multimedia data elements fit in a single cache line, thus improving the relative hit ratio. Finally, it is also possible that the memory behavior of the Berkeley Multimedia Workload component applications have had their memory behavior tuned in order to avoid cache problems.

5.1.2 Multimedia Domains

When broken down into the five application domains (audio, speech, document, video and 3D graphics), some important trends become apparent (Figure 5). Instruction cache miss ratios are quite similar across the various application domains, with a 16 KB or 32 KB cache being sufficient. This supports the idea that multimedia applications are dominated by small kernel loops, rather than large code sizes. Data cache miss ratios show significant variation between domains. Speech, video, and audio domains exhibit similar (low miss ratio) cache performance, while the document and 3D applications have higher miss ratios. This is attributable to the non-linear way in which data sets are traversed during processing for these applications.

5.1.3 SIMD Effects

The motivation behind SIMD within a register approach taken by multimedia extensions such as Intel’s MMX or Motorola’s AltiVec is the fact that on general purpose microprocessors data paths are typically 32 or 64-bits wide, while multimedia applications typically deal with narrower width data. By packing multiple narrow operations into the wider native processor data path, it is possible to improve multimedia performance.

Although it might be expected that current scalar compilers would place multiple short values into a register and then extract them with register to register operations in order to minimize memory access overhead, we found that this was not the case for the compilers available on our DEC Alpha test platform. Instead, multiple independent short loads are issued. Because of this, the use of SIMD instruction set extensions for multimedia will result in higher cache miss ratios, although the total number of memory references would decrease, due to the folding of several scalar load operations into a single parallel operation for sub-word data types which are adjacent in memory. Note that programs employing multimedia (SIMD) instruction sets are likely to be handcoded, as no currently available commercial compilers are able to gen-

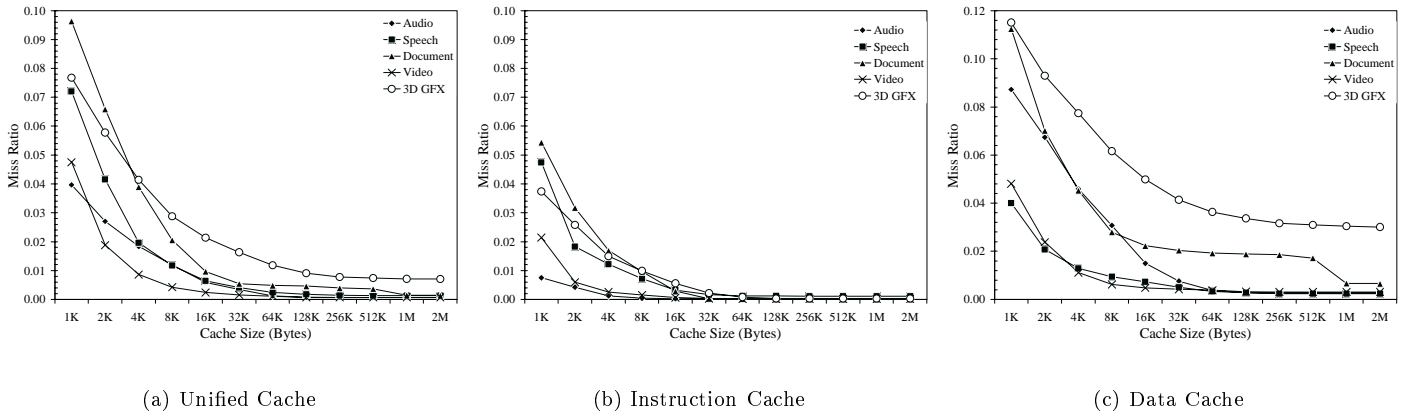


Figure 5: **Multimedia Domains** - Line size is 32 bytes. The domains consist of *3D graphics* (Doom, Mesa, POVray), *document* (Ghostscript, DjVu, JPEG), *audio* (ADPCM, LAME, mpg123, Timidity), *speech* (Rsynth, GSM, Rasta) and *video* (MPEG-2).

erate them automatically; this will also effect their memory behavior.

5.2 Line Size

The block or line size of a cache memory is another cache design parameter that strongly affects cache performance [Smit87]. Generally, increasing the line size decreases the miss ratio, since each fetch from memory retrieves more data, thus fewer accesses outside the cache are required. When the line size is made too large, *memory pollution* can adversely affect cache performance, causing material to be loaded that is either never referenced or evicting information that would have been referenced before being replaced. Large lines also decrease the likelihood of “line crossers” - multibyte memory accesses across the boundary between two cache lines, such as occur with many CISC architectures. This type of access incurs a performance penalty since it usually requires two cache accesses; string operations can induce multiple cache data misses. Additionally, small line sizes require a greater number of bits be dedicated to tag space than for larger lines, although a *sector* or *sub-block* cache is one way to avoid this problem. (See [Roth99a] for an investigation into sub-sector cache design issues.)

In addition to affecting the performance metric of miss ratio, large line sizes can have long transfer times and create excessively high levels of memory traffic [Smit87]. It is possible to model the time to fetch a cache line, t_{line} , assuming no prefetching and that all loads load a full cache line:

$$t_{line} = t_{latency} + \frac{\left(\frac{L}{d}\right)}{r_{xfer}} \quad (1)$$

where,

L - line size (bytes)

d - data path width to memory (bytes)

$t_{latency}$ - delay for any memory transaction, consisting primarily of memory latency and address transmission time (seconds)

r_{xfer} - bus transfer rate or bandwidth (bytes per second)

In order to select an optimal line size, it is necessary to minimize $t_{line} \cdot m(L)$, where $m(L)$ is the miss ratio as a function of line size. To investigate the effect of line size choice on miss ratio, instruction and data caches were simulated with line sizes ranging from 16 bytes to 256 bytes and total capacities ranging from 1 KB to 2 MB. As an example, we used the parameters measured for the memory hierarchy on a 500 MHz AMD Athlon system, as listed in Table 3. Because we are only considering one level caches in this work, we use the measured L2 parameters for the memory miss latency and bandwidth. For every cache capacity there is an optimal line size that minimizes the average memory reference delay. In the case of the largest caches simulated (1M and 2M capacity), the largest line size of 256 bytes produced minimal average delay for instruction caches. Table 6 summarize the mean memory reference delay for the multimedia workload for SPEC92, and SPEC95, in addition to the Berkeley Multimedia Workload. The best values are highlighted in bold text. Some of the instruction cache results exhibit anomalies for extremely small miss ratios due to the limited precision of our results in these instances (only a few misses for many millions of instruction references).

Our results indicate that for the Berkeley Multimedia Workload (as well as SPEC95), instruction cache line sizes should be as large as possible, due to the extremely low miss ratios exhibited for even moderate capacities. Instructions are likely to be accessed sequentially, so the fetching of large line sizes pays off. Data caches, on the other hand, have clearly optimal line sizes, depending on the total cache capacity. In the selection of an optimal line size, it should be kept in mind that large line sizes can be problematic in multiprocessor systems where system bus bandwidth must be shared. Very long line sizes may also cause real-time problems, as when I/O operations cause buffer overruns due to an inability to get on the memory bus. With many desktop computer manufacturers already offering 2 and even 4-way multiprocessor support,

this may have a limiting effect on the usefulness of long cache lines.

5.3 Associativity

Determining optimal associativity is important because changing associativity has a significant impact on cache performance (latency) and cost. Increasing set associativity may require additional multiplexing in the data path as well as increasing the complexity of timing and control [Przy88]. [Hill89] developed a rule of thumb for how associativity affects miss ratio: reducing associativity from eight-way to four-way, from four-way to two-way, and from two-way to direct mapped was found to cause relative miss ratio increases of approximately 5, 10, and 30 percent, respectively. In order to see how associativity affects miss ratios for our multimedia workload, *miss ratio spreads* were calculated for unified, data and instruction caches for our suite of multimedia applications. Miss ratio spread computes the benefit of increasing associativity, and is defined in [Hill89]:

$$Miss\ Ratio\ Spread = \frac{m(A = n) - m(A = 2n)}{m(A = 2n)} \quad (2)$$

Where $m(A = n)$ is the miss ratio for n -way set associativity, A . As in [Hill89], a block size of 32 bytes was chosen, with all simulated caches utilizing the LRU replacement algorithm. The miss ratio spreads of the Berkeley Multimedia Workload as well as SPEC92 and SPEC95 are shown in Figure 6. Please note that in order to preserve visual detail across the wide range of workload behaviors observed, the subfigures use different vertical scales. Unlike the original [Hill89] study, our curves are not smoothed or averaged.

From the miss ratio spread results in Figure 6, we can see that instruction caches for multimedia applications (and generally for SPEC92 and SPEC95) benefit from 2- or 4-way associativity for moderate size caches (16 KB to 256 KB). (Note that the scale is different for each portion of the figure.) For the multimedia workload, most of the benefit from associativity seems to be obtained with two-way set associativity; additional associativity doesn't seem to improve performance significantly, except for small cache sizes. Note that increasing associativity can also be a useful way to increase overall cache capacity when limited by virtual memory constraints (a limited number of page offset bits to index the cache). This was the approach taken both by the designers of Motorola's G4 processor (which includes 8-way associative L1 caches) as well as the IBM 3033 which has a 16-way associative 64k cache.

6 Future Directions

The final determination we would like to make is what cache designers should plan for in order to support future multimedia applications. We look at this in terms of the potential for data set expansion within each multimedia application domain. We expect that audio and speech application data sets will not change significantly in size, as current data sets are already at the limit of human audio fidelity. Document

processing should also not change as current documents are sufficient for either printing or previewing at laser printer resolutions.

Video resolutions are not yet close to the limits of the human eye. This can be seen in the upcoming high resolution digital formats currently in the pipeline for consumer level products: DVD (720x480), HDTV 720P (1280x720), and HDTV 1080I (1920x1080). In order to determine if the working set size of video applications is increasing, and therefore larger cache capacities are necessary to support these new resolutions, we compared the effect of cache capacity on miss ratios for them in Figures 7 and 8 utilizing the ratio of miss ratios for increasing resolution. Our results were obtained by running the same MPEG-2 decoding and encoding applications with three 30 frame data sets at DVD, HDTV 720P and HDTV 1080I resolutions. As an example of how to interpret the figures, DVD⇒720P refers to the ratio of miss ratios of 720P/DVD resolutions. This metric shows the relative change in miss ratio for the higher resolution compared to the preceding lower resolution.

From Figure 7, we can see that instruction miss ratios are hardly affected at all by changes in resolution and although there are some minor fluctuations, the ratios are generally quite close to 1.0. Data miss ratios (Figure 8) show a stronger influence for small caches (capacities less than 32K), but level off for larger caches. This shows that the type of data locality being exploited by data caches for digital video is at the MPEG video block or macroblock level (which are the same size in all formats) rather than the frame level since caches are equally effective on all resolutions above a certain minimum working set size.

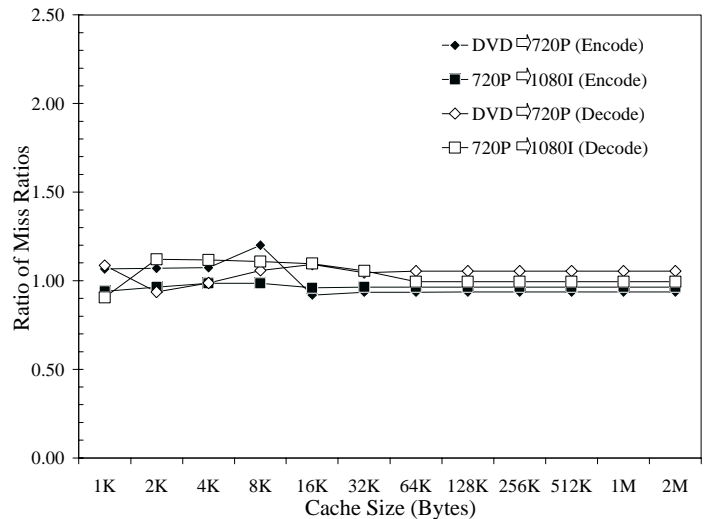


Figure 7: Digital Video Trends: Instruction Cache ratio of miss ratios for increasing resolution

Previous research ([Haku97], [Cox98], [Vart98]) has found that even a small texture cache located on a 3D accelerator board reduces the required bandwidth to main memory significantly. Past architectural trends suggest that all 3D rendering functionality will eventually be folded into the main

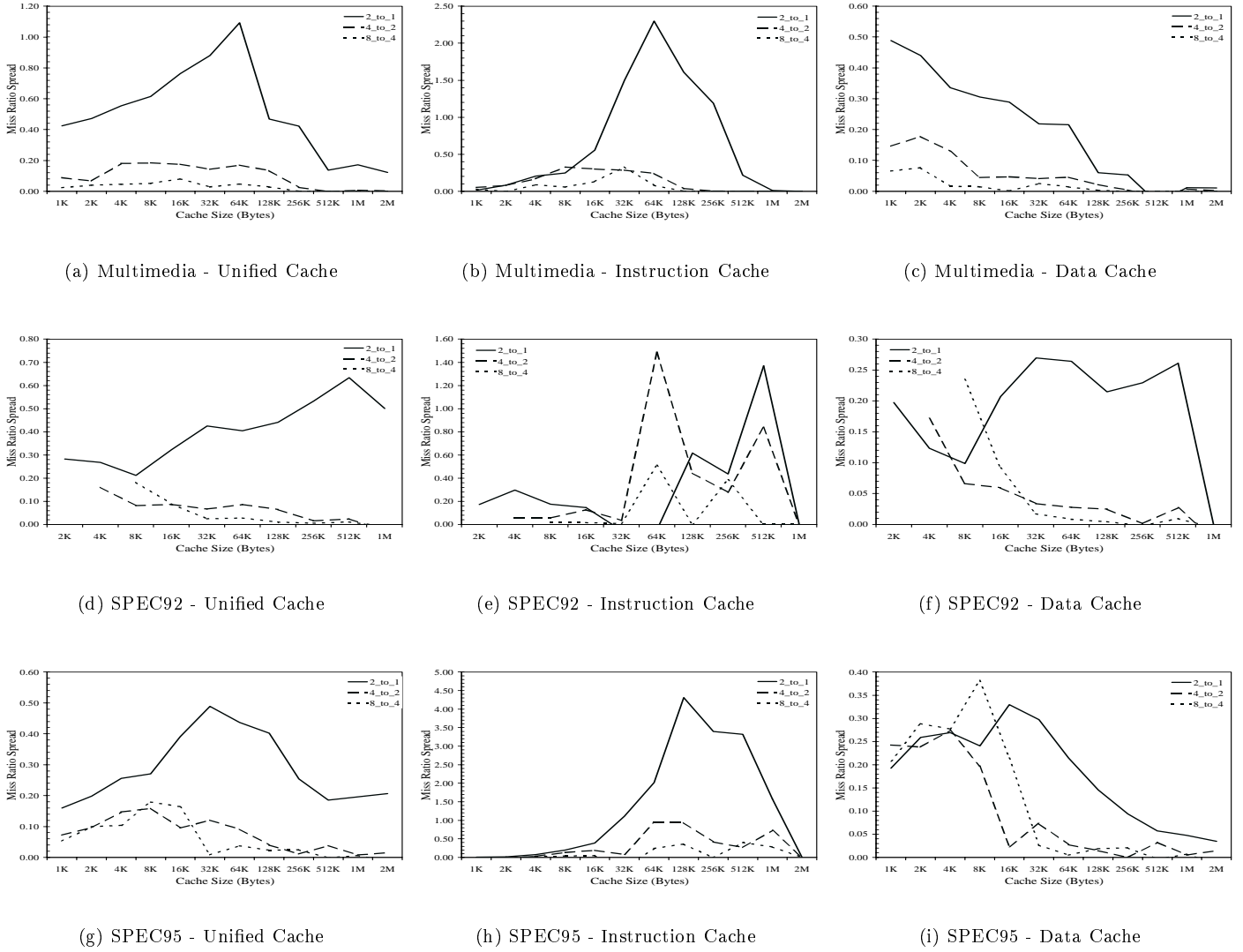


Figure 6: **Berkeley Multimedia, SPEC92 and SPEC95 Miss Ratio Spreads** - Each line, labeled N to M , indicates the fraction increase in miss ratio when reducing associativity from N -way to M -way. To preserve detail across the wide range of workload behaviours observed, different vertical scales are used in each graph.

ogy examined at any cache capacity. Data cache block size selection is more dependent on the capacity of the cache. It is important to note that our block size choices considered only average memory access time, and did not consider issues such as total memory traffic or bus busy periods, which are important considerations for multiprocessor machines.

7.3 Associativity

Based on the results of the miss ratio spread analysis, instruction caches can optimally benefit from 2- or 4-way associativity for most moderate cache sizes (16 KB to 256 KB). Data cache benefits from varying degrees of associativity are more difficult to generalize and appear to be highly dependent on the specific workload, but in general, 2-4 way associativity is also a good choice.

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1 Appendix

1.1 Context Switch Intervals

[Agar88] found that actual multiprogramming traces showed a wide variation in time slice duration and execution order of processes. Although the level of multiprogramming on a desktop workstation is typically low, multimedia applications are often multi-threaded, such that in the example of DVD playback, one thread handles bit stream parsing, another video decoding, and still another audio decoding. Multimedia applications are time dependent; their output or input of processed multimedia data must be synchronized with production or consumption of that data. For this reason, the length of the *context interval* (utilized portion of the quantum) depends on I/O device interaction, number of component threads, and amount of computation time necessary to operate on a given unit of data time.

1.1.1 Windows 2000 Multimedia

In order to estimate typical context switch intervals for real multimedia applications, a set of commercial multimedia applications corresponding to those in the Berkeley Multimedia Workload were measured. All runs were with a single active process running. The context switch intervals of the actual applications from the Berkeley Multimedia Workload were not measured because they are primarily file based applications, typically converting between compressed and uncompressed format without presenting the resulting data to the user. So, although the algorithms they employ (and therefore their memory access patterns) should for the most part be realistically similar to their commercial counterparts, their scheduling behavior is vastly different. For example, in the case of on screen DVD movie play back, there are typically several concurrent threads of execution, each dealing with a particular aspect of MPEG-2 decoding (e.g. audio, video, bitstream parsing/demuxing). Acceptable playback requires that for each unit of data set time each decoding component must be computed:

1. fast enough to leave time for computing the other components in that unit of time (otherwise video frames may need to be dropped)
2. with sufficient precision to not introduce noticeable artifacts
3. within a given time frame to prevent latency effects from disrupting the perceived synchronization between audio and video.

These requirements affect scheduling, and are not taken into account in an application which operates in a batch or offline mode.

Context switch intervals were measured on a 500 MHz AMD Athlon with 256 MB of PC100 DRAM and an MSI MS-6167 motherboard running Windows 2000 Professional v5.00.2195. Both a sound card (Sound Blaster Live Value

and 3D accelerator card (AGP Nvidia Riva TNT) were installed. Table 2 lists these intervals as measured by the Windows 2000 performance counters, which return results in terms of time (CPU cycles).

CINT95	Context Interval
099.go	21,134,208
124.m88ksim	5,122,455
126.gcc	3,845,678
129.compress	22,719,364
130.li	21,754,551
132.jpeg	16,093,926
134.perl	16,308,625
147.vortex	13,193,123

CFP95	Context Interval
101.tomcatv	10,185,364
102.swim	13,753,700
103.su2cor	9,595,431
104.hydro2d	18,624,108
107.mgrid	17,791,106
110.applu	4,644,660
125.turb3d	22,366,853
141.apsi	11,743,787
145.fpppp	19,004,011
146.wave5	19,015,575

Arithmetic Mean	2,243,433
Geometric Mean	2,238,412

Table 1: Average SPEC95 Context Switch Intervals - measurements are given in 500 MHz clock cycles

In our cache simulations, we simulate normal task switching by flushing the cache every $Q_{context}$ instructions. Because our cache simulation is instruction, rather than cycle based, we require cache purge intervals measured in terms of instructions executed between cache flushes. In order to convert our context switch interval data from cycles to instructions we need to know the corresponding cycles per instruction (CPI) ratio. However, we can not simply treat x86 CISC instructions as being equivalent to RISC Alpha instructions, due to the inherently different amounts of work done by each class of instructions. Interestingly, although the x86 instruction set architecture that the AMD Athlon executes is CISC in nature, the full CISC instructions are internally decoded by the Athlon processor into RISC-like instructions referred to as *micro-ops* or simply *ops* [AMD]. Thus, in order to approximate the equivalent number of Alpha RISC-like instructions in each context switch interval, we divide the number of cycles by the number of cycles per micro-op ($CP\mu Op$).

In order to measure a representative value of cycles per micro-op, the same AMD Athlon system as was used to run the Windows workload was measured running the Berkeley Multimedia Workload on Mandrake Linux v7.0. This system was then modified to use kernel version 2.2.15 with Mikael Petterson's perfect counters patch v1.2 [Pett]. The AMD Athlon (as well as many other processors) implement hardware performance counters which can keep track of statistics

Application Name	Data Set	Context Interval
3D Flowerbox OpenGL Screen Saver (Windows 2000)	1280x1024x32bpp, (1:00)	23,653
RealPlayer v7.0 RealAudio Player	KAMU 64Kbps, stereo, G2 stream, (5:00)	40,396
Real Jukebox v1.0.0.488 MP3 Player	Santana - <i>Smooth</i> , 160 Kbps, stereo (4:54)	58,399
MediaPlayer GSM 06.10 (Windows 2000)	Speech by Al Gore, 8 kHz Mono, 16-bits (0:24)	297,641
K-Jofol 2000 MP3 Player v1.0	Santana - <i>Smooth</i> , 160 Kbps, stereo (4:54)	360,336
3D Pipes OpenGL Screen Saver (Windows 2000)	1280x1024x32bpp, (1:00)	567,080
Narrator Text to Speech (Windows 2000)	U.S. Declaration of Independence	594,438
MediaPlayer IMA ADPCM (Windows 2000)	Santana - <i>Smooth</i> , 160 Kbps, stereo (4:54)	708,037
WinDVD v2.0 DVD Player	(5:00) clip from <i>Amadeus</i>	921,510
PowerDVD v2.55 DVD Player	(5:00) clip from <i>Amadeus</i>	1,189,234
Ghostscript/Ghostview PostScript Previewer	Rosenblum and Ousterhaut's LFS paper (15 pages)	1,227,194
Dragon Naturally Speaking Preferred Speech Recognition	U.S. Declaration of Independence	2,560,537
Audio Catalyst v2.1 MP3 Encoder	Santana - <i>Smooth</i> , 44 kHz, stereo (4:54)	3,358,692
Audio Compositor MIDI Renderer	X-files theme song, Personal Copy v4.2 Sound Fonts	3,675,086
Irfanview v3.15 Image Viewer	Kodak's Iowa Corn jpeg image (2048x3072x24bpp)	3,821,284
Quake III Arena (Demo)	Internal demo #1, demo #2 (640x480)	4,284,671
DjVushop Document Compression	Scanned cover of March 2000 <i>IEEE Computer</i> journal	4,754,521
Avi2Mpg2 MPEG-2 Encoder	160 frames, 720x480 from <i>Amadeus</i>	5,339,432
POVray v3.1g Raytracer	Torus (internal demo scene), 800x600 Anti-Aliased	5,928,433
3D Maze OpenGL Screen Saver (Windows 2000)	1280x1024x32bpp, (1:00)	5,930,096
	Arithmetic Mean	2,247,389
	Geometric Mean	1,015,426

Table 2: **Average Multimedia Context Switch Intervals** - Measurements are given in 500 MHz clock cycles. Applications annotated with “(Windows 2000)” are packaged with the Windows 2000 operating system.

such as instructions executed, micro-ops executed, as well as many others [AMD]. (These hardware performance counters are not readily accessible under Windows.) The results of these measurements are shown in Table 3, which lists data both in terms of instructions as well as micro-ops.

In order to determine $Q_{context}$ for the RISC Alpha architecture, we divide the context switch intervals in Table 2 by a CPI equal to the average 1.06 CPμOp measurement from Table 3. As stated earlier, we use this parameter rather than x86 CPI because micro-ops are much more similar to RISC Alpha instructions than CISC x86 instructions. Note also that in a real system the interval between task switches is variable, not fixed; since we don't have the distribution of inter-interrupt times, we chose to use a constant interval. Alternately, we could have chosen some other distribution, such as exponential, normal or uniform.

1.1.2 Compaq Unix SPEC95

Table 1 lists context switch intervals for SPEC95 measured for Compaq Tru64 Unix v5.0 running on a DEC DS20 workstation (dual 21264 processors, each running at 500 MHz), with 2 GB of RAM, again running in a system with a single active task. For comparison, we review below the multiprogramming parameters of a variety of other workloads and systems previously studied in the literature. [Agar88] found that task switch times varied between 10,000 and 50,000 instruction references for both DEC Ultrix and VMS operating systems on a VAX 8200 processor (5 MHz). [Borg90] lists parameters

for Titan, an experimental RISC workstation with a clock speed of 22.2 MHz, for which $Q = 25,000$ clock cycles, with CPI typically being greater than one. [Clark83] measured context switch intervals between 11,000 and 23,000 instruction references on the DEC VAX 11/780 (5 MHz). Later measurements by the same author in [Clark88] on a VAX 8800 processor (22.2 MHz) found an average of 19,353 instructions between context switches. The traces used in [Smit87] were from a variety of architectures (Zilog Z8000, DEC VAX 11/780, CDC 6400, IBM 370, and Motorola 68000), and were simulated with a task switch interval of 15,000 – 20,000 memory references. [Koba86] examines the task switching behavior of IBM's MVS operating system (OS/VS2 MVS) on an Amdahl 470 V/8 system. Measurements obtained by a hardware monitor for a production time sharing option (TSO) workload had task intervals of approximately 7,600 instructions and 3,600 instructions for supervisor (system) state and problem (user) state respectively. A batch workload exhibited 8,700 and 14,000 for supervisor and problem state. Note that all of these other workloads were heavily multiprogrammed (and timeshared), and thus are not fully comparable. Of course, much computation is currently done on single user PCs and workstations, so a uniprogrammed system is probably the most representative of current technology.

1.2 Simulation Methodologies

Even though our study utilizes execution driven simulation, tracing full applications is still costly in terms of simulation

Name	User Time (cycles)	Instructions	Micro-Ops	Cycles/Instruction	Cycles/Micro-Op
ADPCM Encode	76,904,958	61,876,844	62,158,059	1.24	1.24
ADPCM Decode	64,344,819	53,313,197	53,594,784	1.21	1.20
DJVU Encode	445,708,199	287,174,703	322,253,494	1.55	1.38
DJVU Decode	356,305,000	244,918,278	266,984,846	1.45	1.33
Doom	1,472,798,700	793,162,073	1,181,637,518	1.86	1.25
Ghostscript	670,630,530	748,440,530	827,890,835	0.90	1.81
GSM Encode	188,190,001	225,158,845	248,092,796	0.84	0.76
GSM Decode	60,417,117	83,563,455	87,869,424	0.72	0.69
JPEG Encode	153,366,654	155,941,646	172,197,756	0.98	0.89
JPEG Decode	78,532,637	69,994,886	71,219,757	1.12	1.10
LAME	10,695,164,749	8,758,744,400	9,792,965,536	1.22	1.09
Mesa Gears	607,508,141	238,630,536	246,478,641	2.55	2.46
Mesa Morph3D	430,137,133	200,480,866	247,112,920	2.15	1.74
Mesa Reflect	1,940,806,991	1,692,447,264	2,090,552,059	1.15	0.93
MPEG-2 Encode DVD	14,037,454,521	14,005,949,265	16,702,192,536	1.00	0.84
MPEG-2 Encode 720P	37,759,708,362	37,445,342,666	44,698,434,032	1.01	0.84
MPEG-2 Encode 1080I	85,720,663,990	87,173,068,231	103,429,470,721	0.98	0.83
MPEG-2 Decode DVD	778,728,056	930,444,099	974,763,847	0.84	0.80
MPEG-2 Decode 720P	2,462,187,286	2,937,962,420	3,110,807,374	0.84	0.79
MPEG-2 Decode 1080I	5,043,716,605	5,759,111,626	6,014,852,989	0.88	0.84
mpg123	446,758,849	409,577,365	486,650,398	1.09	0.92
POVray3	72,427,881,123	5,137,007,093	6,809,522,382	1.45	1.09
Rasta	27,180,004	21,569,326	26,527,625	1.26	1.02
Rsynth	526,040,697	421,248,076	534,184,372	1.25	0.98
Timidity	1,132,954,552	1,363,791,599	1,522,840,735	0.83	0.74
Average				1.21	1.06

Table 3: Measured CPI and $CP\mu Op$ for Berkeley Multimedia Workload - 500 MHz AMD Athlon system, 128 MB RAM, running Mandrake Linux v7.0 with a modified kernel v2.2.15

time. Our cache simulations were run on a lab of twenty Alpha AXP 300 workstations at Berkeley, each with a single 300 MHz Alpha 21064a processor and 128 MB of RAM. Simulation time per memory reference is dependent on the type of cache being simulated, requiring $0.418 \mu s$ (126 cycles), $1.770 \mu s$ (531 cycles), and $1.262 \mu s$ (379 cycles) on average per reference for instruction, data and unified cache simulations respectively. Instruction cache simulation is especially fast because references can be simulated at the basic block level of granularity rather than per instruction as is necessary for data references. Average simulation time per reference was between $0.114 \mu s$ (35 cycles) and $2.112 \mu s$ (634 cycles) (for comparison, [Gee93]’s simulation of SPEC92 on 40 MHz DECstation 5000/240 machines required $200 \mu s$ (8000 cycles) to $400 \mu s$ (16,000 cycles) per reference simulated for simulations). Total simulation time for our work, not including false starts, machine down time and other simulation problems was 24.4 days of CPU time for each multimedia run (once with and once without multiprogramming), and 147.2 days of CPU time for SPEC95 simulations, for a grand total of 196 days of CPU time.

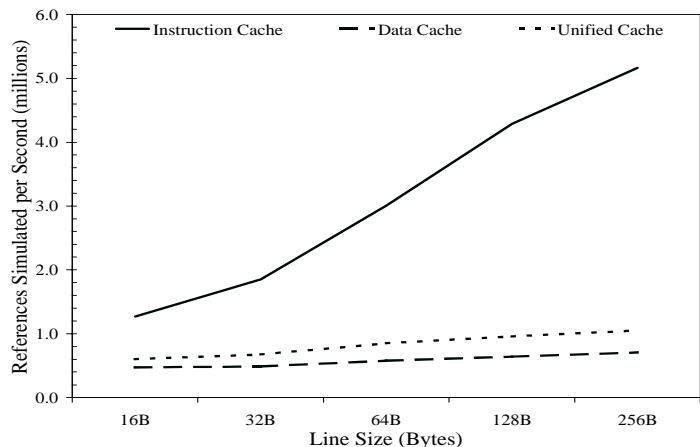


Figure 1: Average ATOM Cheetah Simulation Speeds

1.3 Current Cache Configurations

As can be seen from Table 4, currently available processors are very similar in their cache design choices.

	AMD Athlon	DEC 21264A	HP PA-8500	Intel Pentium III	MIPS R12000	Motorola 7400 (G4)	Sun UltraSPARC Iii
Transistors ($\times 10^6$)	22	15.2	140	9.5	6.9	6.5	5.4
Process (μm)	0.25	0.25	0.25	0.18	0.25	0.20	0.25
Die Size (mm^2)	184	205	468.6	104.6	204	83	126
Clock (MHz)	800	750	440	733	300	500	480
L1 \$I\$ Size (KB)	64	64	512	16	32	32	16
L1 \$I\$ Associativity	2	2	4	4	2	8	2
L1 \$I\$ Line Size (bytes)	64	16	32/64	32	32	32	32
L1 \$D\$ Size (KB)	64	64	1024	16	32	32	16
L1 \$D\$ Associativity	2	2	4	4	2	8	1
L1 \$D\$ Line Size (bytes)	64	64	32/64	32	32	32	32

Table 4: Current Microprocessor Cache Configurations [Burd][Noer]

1.4 Measuring Cache Parameters

In order to choose the optimal line size for a given cache size, it is first necessary to know the parameters of the memory system to be used. In order to illustrate this, we employed HBench-OS v1.0 [Brow97], an extended version of the lmbench micro-benchmarking suite detailed in [McVoy96] (this work was apparently developed independently from the TLB and cache measurement techniques presented in [Saav95]). Each micro-benchmark measures the average time per iteration required to read or write a subset of elements belonging to an array of known size. The number of cache misses (and therefore the latency) is a function of the size of the array and the stride between consecutive addresses referenced. This effect can be seen in Figure 2 which graphs latency for various stride sizes for the 500 MHz AMD Athlon system utilized in our study. Each data set curve represents a stride size with the array size varying from 512 bytes up to 8 Mbytes, with a latency of 1 clock cycle taken to be “zero” - the time reported is only memory latency time, and does not include the instruction execution time. This is why all of the curves in Figure 2 are zero left of the L1 data cache capacity (64 Kbytes). Each horizontal plateau represents another level of the memory hierarchy (L1 at 64 Kbytes, L2 at 512 Kbytes for the AMD Athlon). Different strides are measured by the benchmark in order to determine the cache line size. The smallest stride that has a latency equal to that of main memory is the cache line size because the strides that are faster than memory must necessarily hit more than once per cache line.

1.5 Comparison with [Smit87]

In order to compare our line size analysis results with other workloads, we examined the metric of *ratio of miss ratios* [Smit87], which is the ratio of the miss ratio at a given cache size and line size to that for the same cache size but half the line size. The analysis of line size in [Smit87] employs a set of 27 traces from five different machine architectures. Table 5 compares the ratio of miss ratios metric for that workload against those of our multimedia workload. Graphs of the ratios of miss ratios for the Berkeley Multimedia Workload

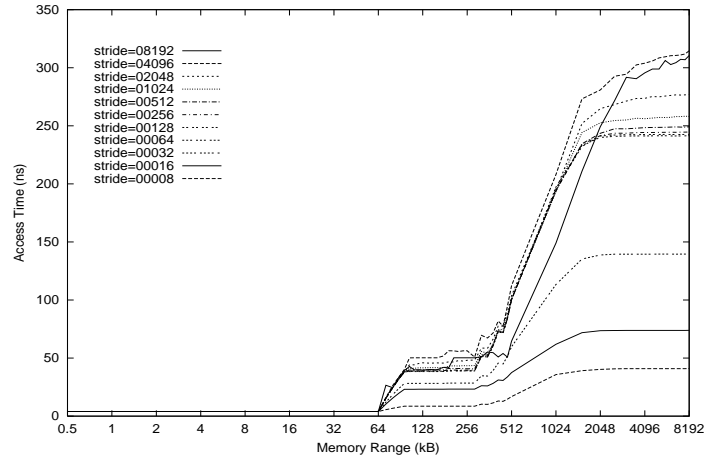


Figure 2: 500 MHz Athlon System Memory Latency Profile - memory latency for various stride length memory accesses

are shown in Figures 3, 4, and 5. Cache behavior was quite similar between the two workloads except in the case of data caches. The multimedia workload benefitted more than the one studied in [Smit87] when going from 16B to 32B data cache line lengths, but the opposite held true for the other data cache line length comparisons (64B:32B and 128B:64B).

1.6 CCC Model

It is useful to examine the miss ratio spreads for the multimedia, SPEC92 and SPEC95 workloads in light of the three C’s model of cache miss behavior introduced in [Hill87] which categorizes misses into three classes: *conflict misses*, which are due to two different elements of the working set mapping to the same physical cache blocks (none for a fully associative cache), *capacity misses* which result from the cache capacity being too small to hold the working set (none for an infinitely large cache) and *compulsory misses* which are necessary when initially loading the cache (present for any cache configuration). It is only where conflict misses exist that associativity makes a difference, and there is a great variation among different applications in the contribution conflict misses make

32B:16B						
	Unified		Instruction		Data	
Size	Media	[Smit87]	Media	[Smit87]	Media	[Smit87]
1K	0.676	0.831	0.597	0.963	0.789	0.836
2K	0.679	0.731	0.607	0.737	0.670	0.787
4K	0.727	0.719	0.673	0.651	0.657	0.727
8K	0.654	0.645	0.622	0.598	0.627	0.667
16K	0.627	0.616	0.609	0.581	0.633	0.646
32K	0.632	0.601	0.559	0.581	0.615	0.646
64B:32B						
	Unified		Instruction		Data	
Size	Media	[Smit87]	Media	[Smit87]	Media	[Smit87]
2K	0.819	0.787	0.698	0.701	0.889	0.853
4K	0.785	0.746	0.831	0.660	0.740	0.770
8K	0.756	0.661	0.717	0.667	0.706	0.723
16K	0.676	0.633	0.633	0.624	0.662	0.672
32K	0.656	0.601	0.696	0.624	0.686	0.662
128B:64B						
	Unified		Instruction		Data	
Size	Media	[Smit87]	Media	[Smit87]	Media	[Smit87]
4K	0.938	1.809	0.733	0.831	0.925	0.835
8K	0.937	0.753	0.776	0.690	0.865	0.817
16K	0.868	0.685	0.655	0.657	0.841	0.747
32K	0.739	0.660	0.854	0.634	0.750	0.697

Table 5: Comparison to [Smit87] - Ratio of miss ratio to that of line half as long. Results are shown only for those cache configurations that are common to both [Smit87] and this study.

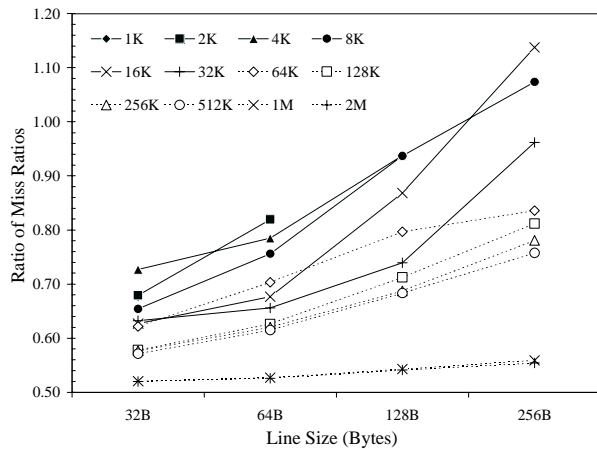
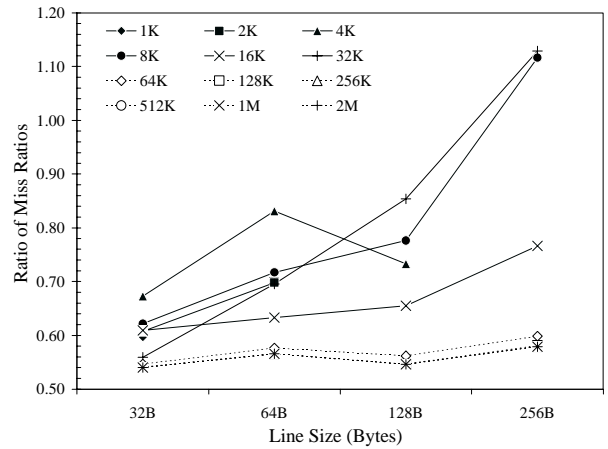


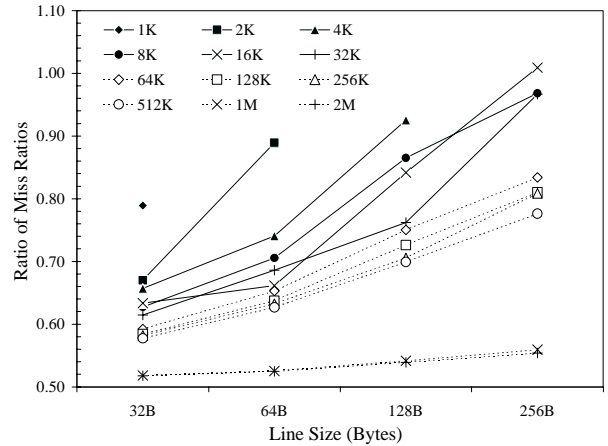
Figure 3: Ratio of Miss Ratios: Unified Cache - Berkeley Multimedia Workload

to overall miss ratio. Figure 6 graphs the variation of the three types of misses for MPEG decoding at DVD resolution, and the SPECint95 147.vortex application. What is clear is that these two applications have widely different proportions of conflict, capacity and compulsory miss ratios for any given cache capacity. Although individual traces exhibit widely differing contributions from the three miss ratio factors, traces



(a) Instruction Cache

Figure 4: Ratio of Miss Ratios: Instruction Cache - Berkeley Multimedia Workload



(a) Data Cache

Figure 5: Ratio of Miss Ratios: Data Cache - Berkeley Multimedia Workload

on average follow the heuristics of [Hill89] (see Figure 7).

1.7 Workloads

1.7.1 SPEC92 [Gee93]

In the past decade, SPEC (Standard Performance Evaluation Corporation) benchmarks have played an extremely important role in both hardware and compiler design. SPEC CPU benchmarks are taken to be generally representative of traditional workstation applications, with the integer component reflecting system or commercial applications, and the floating point component representing numeric and scientific applications. The SPEC92 benchmark consists of six integer-

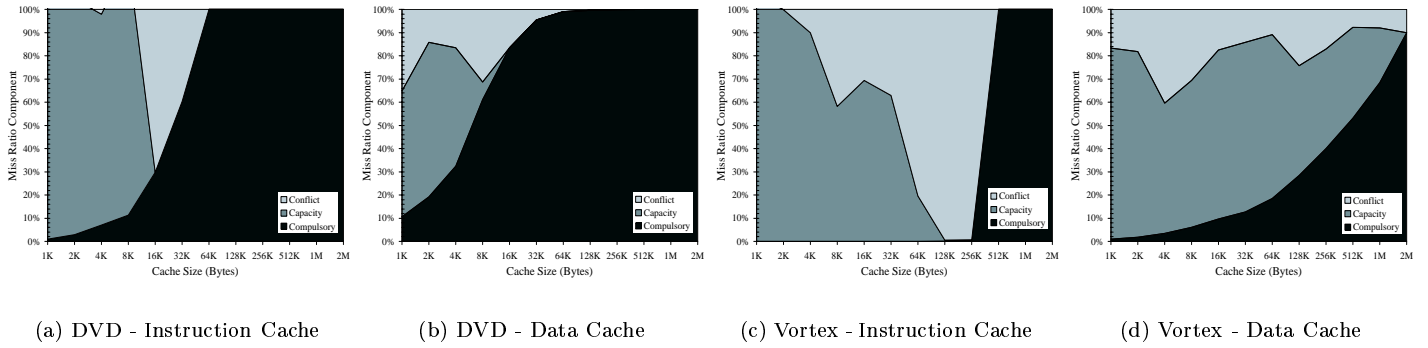


Figure 6: Miss Ratio Factors

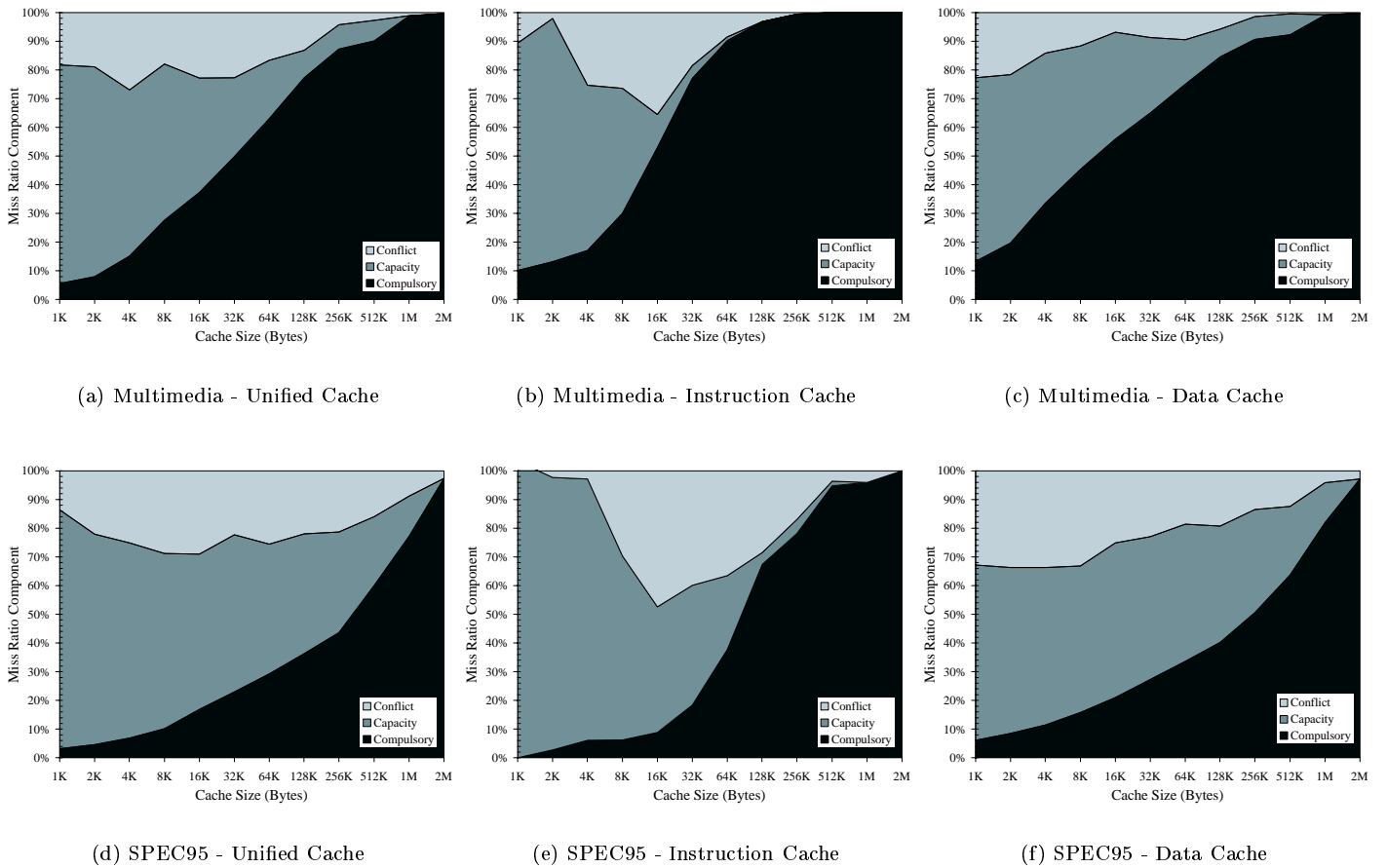


Figure 7: Average Miss Ratio Factors

intensive, and fourteen floating-point-intensive programs (see Table 6). All of the component benchmarks are written in either C (integer) or Fortran (floating point).

It is important to note that although the SPEC component applications are based on real world counterparts, many of them were modified by SPEC from their original form to reduce the influence of I/O and the operating system on performance. In some instances, this means that test data is read from and written to memory, rather than disk (as would be the case in the original form of the application). Clearly this

could potentially affect memory behavior compared to real world applications.

[Gee93] analyzed the cache behavior of the SPEC92 benchmark suite running on DECstations with MIPS R2000 or R3000 processors and version 4.1 of the DEC Ultrix operating system. Version 2.0 of the C compiler and version 2.1 of the FORTRAN compiler were used with the optimization level according to the SPEC Makefiles. Because the SPEC benchmarks are typically run in a uniprogrammed environment, no cache flushing or other method was used to simulate

multiprogramming. [Gee93] also found that for the SPEC92 benchmark suite, system time is insignificant compared to user time, and so operating system memory behavior is largely unimportant for this suite of applications.

Integer	Description
008.espresso	Circuit theory
022.li	Lisp interpreter
023.eqntott	Logic design
026.compress	Lempel-Ziv coding
072.sc	Spread sheet
085.gcc	GNU C Compiler
Floating Point	Description
013.spice2g6	Circuit design
015.doduc	Monte-Carlo simulation
034.mdljdp2	Quantum chemistry
039.wave5	Maxwell's equations
047.tomcatv	Coordinate translation
048.ora	Optics ray-tracing
052.alvinn	Robotics
056.ear	Model of the human ear
077.mdljsp2	Quantum chemistry
078.swm256	Shallow water model
089.su2cor	Quantum physics
090.hydro2d	Astrophysics
093.nasa7	NASA kernels
094.fpppp	Quantum chemistry

Table 6: SPEC92 Benchmark Suite

1.7.2 SPEC95

SPEC95 is an upgraded version of the SPEC92 benchmark suite. It consists of eight integer intensive and ten floating-point intensive applications. Several of the programs from SPEC92 are found in SPEC95. 126.gcc is the same as 085.gcc except that a newer version of gcc is used. 129.compress is the same as 026.compress. 130.li is the same as 022.li. 101.tomcatv is the same as 047.tomcatv. 102.swim is the same as 078.swm256 except that it uses a 1024x1024 grid. 103.su2cor is the same as 089.su2cor. 104.hydro2d is the same as 090.hydro2d. 145.fpppp is the same as 094.fpppp. 146.wave5 is the same as 039.wave5. In general, the applications were designed to have larger code size and greater memory activity than those of SPEC92.

1.7.3 Multiprogramming Workload (Mult) [Borg90]

[Borg90] generated miss ratios for very long address traces (up to 12 billion memory references in length) on the Titan RISC architecture in order to evaluate the performance of a variety of cache designs. Three individual traces were used in addition to another which was a multiprogrammed workload consisting of several jobs. Our comparison includes their miss ratio results for their 7.6 billion reference (68.5% instruction, 30.6% load, 15.4% store) multiprogramming workload

(referred to as “Mult” by the authors of [Borg90]). It consists of:

- make run compiling (from C) portions of the magic source code
- grr routing the DECstation 3100 printed circuit board
- magic (VLSI editor) design rule checking the MultiTitan CPU chip
- tree (compiled Scheme) builds tree data structure and searches for largest element
- make run that calls xld (linker/loader) on the magic code
- tcsh script of infinite loop of interactive commands (cp, cat, ex, rm, ps, -aux, ls -l /*)

1.7.4 Design Target Miss Ratios (DTMR) [Smit85]

[Smit85] introduced the concept of *design target miss ratios* (DTMRs), intended to represent typical levels of performance across a wide class of workloads and machines, to be used for hardware design. The DTMRs were synthesized from real (hardware monitor) measurements that existed in the literature and from trace driven simulations using a large number of traces taken from several architectures, originally coded in several different languages.

1.7.5 VAX 11/780 [Clark83], VAX 8800 [Clark88]

Two studies done at Digital Equipment Corporation (DEC) supply miss ratios for a time-shared engineering workload taken with a hardware monitor on VAX 11/780 and VAX 8800 machines [Clark83], [Clark88]. The 11/780 has an 8-KB, write through, unified cache with an 8-byte block size and associativity of two. The 8800 has a 64-KB, write-through, direct mapped, unified cache with a 64-byte block size. On the VAX 11/780 it is possible to disable half of the two-way associative cache through special control bits; a technique which allowed for measurement of a 4-KB, direct mapped, unified cache configuration as well.

1.7.6 Agarwall Mul3 [Agar88]

In [Agar88] an analysis of the effect of operating system references and multiprogramming was presented for a workload of eleven application programs (30 traces in all). The platform used to gather the traces was a VAX 11/780 running either the Ultrix or VMS operating system. All of the traces were gathered through the ATUM scheme of microcode modification, and were roughly 400,000 references long (approximately half a second of execution time). A technique termed *trace sampling* was used to concatenate smaller traces to better simulate the full trace length of a running program. We utilize their three way multiprogrammed workload for comparison.

Integer	Description	Instruction	Load	Store
099.go	AI plays "Go"	32,465,547,697	8,168,233,239	2,409,111,305
124.m88ksim	Motorola 88K simulator	73,820,020,885	13,680,509,709	7,402,458,586
126.gcc	GCC, builds SPARC code	209,948,942	49,135,874	24,970,849
129.compress	Lempel-Ziv coding	60,850,564,695	11,722,190,689	4,458,902,946
130.li	Lisp interpreter	65,730,724,167	16,730,950,984	9,385,736,837
132.jpeg	DCT image compression	34,116,845,423	6,023,880,310	1,870,937,674
134.perl	Anagrams/primes in Perl	29,378,239,506	6,868,627,321	4,173,646,937
147.vortex	Database	87,529,422,776	20,621,987,100	11,989,029,595
Floating Point	Description			
101.tomcatv	Mesh generation	31,932,871,503	6,481,320,753	3,324,212,603
102.swim	Shallow water model	32,575,361,567	5,702,422,493	2,773,604,570
103.su2cor	Monte Carlo simulation	39,599,980,228	7,061,086,677	3,214,956,672
104.hydro2d	Hydrodynamical Eqns	48,836,577,610	10,074,625,107	3,468,630,651
107.mgrid	Multigrid solver in 3D field	72,429,596,913	18,187,911,190	3,911,599,079
110.applu	Differential equations	33,716,422,315	7,722,618,047	3,267,428,916
125.turb3d	Turbulence in cube	104,351,000,000	15,919,035,949	13,253,927,515
141.apsi	Temp, Wind, Potential	33,155,694,301	6,254,642,763	3,445,287,831
145.fpppp	Quantum chemistry	147,327,000,000	43,911,029,435	11,283,084,727
146.wave5	Plasma physics	34,209,423,864	6,831,165,556	4,455,048,459
Total		962,235,242,392	212,011,373,196	94,112,575,752
Arithmetic Mean		53,457,513,466	11,778,409,622	5,228,476,431

Table 7: SPEC95 Benchmark Suite Characteristics

1.7.7 Amdahl 470 [Smit82]

In [Smit82], hardware monitor measurements taken at Amdahl Corporation on Amdahl 470V machines are presented. A standard internal benchmark was run containing supervisor, commercial and scientific code. Supervisor state miss ratios were found to be much higher than problem state miss ratios.

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Berkeley Multimedia Workload

Multimedia					
Instruction Cache					
Associativity					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.05622	0.05594	0.05259	0.05103	0.05180
2K	0.02969	0.02845	0.02561	0.02622	0.02664
4K	0.01850	0.01506	0.01316	0.01140	0.01046
8K	0.01128	0.00861	0.00668	0.00598	0.00544
16K	0.00637	0.00390	0.00298	0.00280	0.00285
32K	0.00377	0.00151	0.00119	0.00093	0.00075
64K	0.00274	0.00089	0.00074	0.00069	0.00068
128K	0.00163	0.00069	0.00067	0.00067	0.00067
256K	0.00128	0.00068	0.00067	0.00067	0.00067
512K	0.00077	0.00067	0.00067	0.00067	0.00067
1M	0.00068	0.00067	0.00067	0.00067	0.00067
2M	0.00067	0.00067	0.00067	0.00067	0.00067
Data Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.12894	0.09619	0.08640	0.08325	0.08019
2K	0.09326	0.07223	0.06574	0.06360	0.06244
4K	0.06587	0.05530	0.05154	0.05108	0.05102
8K	0.04903	0.04176	0.04092	0.04068	0.04067
16K	0.03762	0.03131	0.02995	0.02996	0.02994
32K	0.02924	0.02527	0.02432	0.02381	0.02365
64K	0.02556	0.02194	0.02131	0.02112	0.02099
128K	0.02154	0.02074	0.02046	0.02047	0.02048
256K	0.02079	0.02011	0.02002	0.02000	0.01999
512K	0.01932	0.01966	0.01982	0.01981	0.01981
1M	0.01756	0.01744	0.01736	0.01737	0.01737
2M	0.01746	0.01734	0.01732	0.01732	0.01732
Unified Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.11725	0.09241	0.08662	0.08609	0.08794
2K	0.07795	0.05897	0.05644	0.05513	0.05451
4K	0.05180	0.03546	0.03112	0.02913	0.02860
8K	0.03314	0.02224	0.01923	0.01851	0.01780
16K	0.02215	0.01388	0.01197	0.01148	0.01141
32K	0.01613	0.00954	0.00841	0.00826	0.00836
64K	0.01254	0.00677	0.00590	0.00562	0.00546
128K	0.00776	0.00549	0.00509	0.00502	0.00501
256K	0.00652	0.00499	0.00490	0.00490	0.00489
512K	0.00524	0.00484	0.00482	0.00481	0.00481
1M	0.00471	0.00432	0.00430	0.00430	0.00430
2M	0.00463	0.00430	0.00429	0.00429	0.00429

Block Size: 16 bytes

Audio					
Instruction Cache					
Associativity					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.01575	0.01348	0.01284	0.01274	0.01277
2K	0.00770	0.00722	0.00758	0.00776	0.00781
4K	0.00240	0.00212	0.00223	0.00221	0.00216
8K	0.00093	0.00074	0.00070	0.00072	0.00071
16K	0.00060	0.00046	0.00032	0.00028	0.00027
32K	0.00037	0.00028	0.00028	0.00026	0.00026
64K	0.00034	0.00026	0.00026	0.00026	0.00026
128K	0.00026	0.00026	0.00026	0.00026	0.00026
256K	0.00026	0.00026	0.00026	0.00026	0.00026
512K	0.00026	0.00026	0.00026	0.00026	0.00026
1M	0.00026	0.00026	0.00026	0.00026	0.00026
2M	0.00026	0.00026	0.00026	0.00026	0.00026
Data Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.16773	0.12483	0.11573	0.11242	0.11204
2K	0.12176	0.10471	0.10424	0.10325	0.10329
4K	0.08938	0.07868	0.07853	0.07833	0.07821
8K	0.05846	0.05305	0.05281	0.05375	0.05397
16K	0.03739	0.02686	0.02336	0.02407	0.02496
32K	0.01788	0.01419	0.01347	0.01299	0.01309
64K	0.01026	0.00698	0.00658	0.00617	0.00564
128K	0.00653	0.00530	0.00518	0.00517	0.00516
256K	0.00619	0.00516	0.00515	0.00515	0.00515
512K	0.00532	0.00514	0.00514	0.00514	0.00514
1M	0.00515	0.00514	0.00514	0.00514	0.00514
2M	0.00515	0.00514	0.00514	0.00514	0.00514
Unified Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.08687	0.05124	0.04419	0.04235	0.04191
2K	0.05540	0.03974	0.03559	0.03488	0.03452
4K	0.04166	0.02996	0.02793	0.02746	0.02730
8K	0.02723	0.02010	0.01998	0.02089	0.02127
16K	0.01634	0.01014	0.00821	0.00832	0.00861
32K	0.00896	0.00600	0.00427	0.00392	0.00390
64K	0.00591	0.00232	0.00214	0.00200	0.00208
128K	0.00454	0.00141	0.00127	0.00126	0.00125
256K	0.00154	0.00127	0.00124	0.00124	0.00124
512K	0.00133	0.00124	0.00124	0.00124	0.00124
1M	0.00127	0.00124	0.00124	0.00124	0.00124
2M	0.00127	0.00124	0.00124	0.00124	0.00124

Speech					
Instruction Cache					
Associativity					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.08537	0.08410	0.07580	0.06868	0.06710
2K	0.03110	0.03111	0.02533	0.02497	0.02509
4K	0.02261	0.01934	0.01925	0.02011	0.02117
8K	0.01311	0.01093	0.00856	0.00726	0.00698
16K	0.00773	0.00534	0.00434	0.00460	0.00469
32K	0.00387	0.00292	0.00256	0.00222	0.00213
64K	0.00312	0.00222	0.00215	0.00210	0.00210
128K	0.00236	0.00215	0.00210	0.00210	0.00210
256K	0.00225	0.00210	0.00210	0.00210	0.00210
512K	0.00210	0.00210	0.00210	0.00210	0.00210
1M	0.00210	0.00210	0.00210	0.00210	0.00210
2M	0.00210	0.00210	0.00210	0.00210	0.00210
Data Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.07101	0.03968	0.03498	0.03365	0.03282
2K	0.04576	0.02355	0.02034	0.01958	0.01915
4K	0.02472	0.01564	0.01433	0.01336	0.01323
8K	0.01810	0.01306	0.01203	0.01196	0.01194
16K	0.01261	0.01059	0.01052	0.01107	0.01139
32K	0.00831	0.00670	0.00645	0.00565	0.00534
64K	0.00646	0.00510	0.00444	0.00432	0.00428
128K	0.00502	0.00460	0.00425	0.00423	0.00423
256K	0.00434	0.00423	0.00422	0.00422	0.00422
512K	0.00424	0.00422	0.00422	0.00422	0.00422
1M	0.00422	0.00422	0.00422	0.00422	0.00422
2M	0.00422	0.00422	0.00422	0.00422	0.00422
Unified Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.13689	0.10809	0.10562	0.10710	0.10917
2K	0.08654	0.06400	0.06637	0.06477	0.06461
4K	0.05718	0.02865	0.02468	0.02439	0.02443
8K	0.03182	0.01647	0.01357	0.01323	0.01254
16K	0.02403	0.00965	0.00753	0.00674	0.00668
32K	0.01900	0.00628	0.00579	0.00586	0.00613
64K	0.01583	0.00390	0.00329	0.00323	0.00280
128K	0.00421	0.00306	0.00263	0.00255	0.00255
256K	0.00379	0.00257	0.00255	0.00255	0.00255
512K	0.00286	0.00255	0.00255	0.00255	0.00255
1M	0.00286	0.00255	0.00255	0.00255	0.00255
2M	0.00286	0.00255	0.00255	0.00255	0.00255

Table 8: Average Miss Ratios for Berkeley Multimedia Workload (16 byte Block Size)

Berkeley Multimedia Workload

Block Size: 32 bytes

Multimedia						Audio						Speech					
Instruction Cache						Instruction Cache						Instruction Cache					
Associativity						Associativity						Associativity					
Size	Direct	2-way	4-way	8-way	16-way	Size	Direct	2-way	4-way	8-way	16-way	Size	Direct	2-way	4-way	8-way	16-way
1K	0.03410	0.03361	0.03194	0.03103	0.03091	1K	0.00912	0.00750	0.00715	0.00711	0.00713	1K	0.04958	0.04738	0.04289	0.03847	0.03735
2K	0.01865	0.01720	0.01594	0.01600	0.01618	2K	0.00480	0.00427	0.00425	0.00417	0.00421	2K	0.01913	0.01830	0.01505	0.01467	0.01469
4K	0.01155	0.00958	0.00818	0.00751	0.00704	4K	0.00142	0.00122	0.00120	0.00120	0.00117	4K	0.01372	0.01219	0.01219	0.01224	0.01247
8K	0.00718	0.00575	0.00433	0.00410	0.00338	8K	0.00054	0.00043	0.00040	0.00040	0.00043	8K	0.00814	0.00724	0.00596	0.00516	0.00479
16K	0.00388	0.00250	0.00192	0.00169	0.00173	16K	0.00034	0.00026	0.00019	0.00016	0.00015	16K	0.00456	0.00321	0.00250	0.00259	0.00258
32K	0.00229	0.00092	0.00071	0.00054	0.00042	32K	0.00021	0.00015	0.00015	0.00014	0.00014	32K	0.00235	0.00169	0.00147	0.00125	0.00118
64K	0.00167	0.00051	0.00041	0.00038	0.00037	64K	0.00019	0.00014	0.00014	0.00014	0.00014	64K	0.00179	0.00122	0.00115	0.00112	0.00112
128K	0.00099	0.00038	0.00037	0.00036	0.00036	128K	0.00014	0.00014	0.00014	0.00014	0.00014	128K	0.00129	0.00116	0.00112	0.00112	0.00112
256K	0.00080	0.00037	0.00036	0.00036	0.00036	256K	0.00014	0.00014	0.00014	0.00014	0.00014	256K	0.00121	0.00112	0.00112	0.00112	0.00112
512K	0.00044	0.00036	0.00036	0.00036	0.00036	512K	0.00014	0.00014	0.00014	0.00014	0.00014	512K	0.00112	0.00112	0.00112	0.00112	0.00112
1M	0.00037	0.00036	0.00036	0.00036	0.00036	1M	0.00014	0.00014	0.00014	0.00014	0.00014	1M	0.00112	0.00112	0.00112	0.00112	0.00112
2M	0.00036	0.00036	0.00036	0.00036	0.00036	2M	0.00014	0.00014	0.00014	0.00014	0.00014	2M	0.00112	0.00112	0.00112	0.00112	0.00112

Table 9: Average Miss Ratios for Berkeley Multimedia Workload (32 byte Block Size)

Berkeley Multimedia Workload

Block Size: 128 bytes

Multimedia							Audio							Speech							
Instruction Cache							Instruction Cache							Instruction Cache							
Associativity							Associativity							Associativity							
Size	Direct	2-way	4-way	8-way	16-way		Size	Direct	2-way	4-way	8-way	16-way		Size	Direct	2-way	4-way	8-way	16-way		
1K	0.01738	0.01599	0.01564				1K	0.00347	0.00291	0.00310				1K	0.02762	0.02146	0.01861				
2K	0.00938	0.00828	0.00831	0.00842			2K	0.00209	0.00148	0.00145	0.00130			2K	0.00818	0.00722	0.00620	0.00648			
4K	0.00581	0.00491	0.00455	0.00422	0.00429		4K	0.00062	0.00054	0.00045	0.00046	0.00047		4K	0.00581	0.00522	0.00499	0.00490	0.00490		
8K	0.00382	0.00293	0.00256	0.00260	0.00188		8K	0.00022	0.00017	0.00015	0.00015	0.00016		8K	0.00385	0.00349	0.00381	0.00409	0.00415		
16K	0.00203	0.00127	0.00102	0.00073	0.00072		16K	0.00013	0.00009	0.00007	0.00006	0.00006		16K	0.00196	0.00144	0.00121	0.00088	0.00087		
32K	0.00124	0.00047	0.00034	0.00030	0.00025		32K	0.00008	0.00005	0.00005	0.00004	0.00004		32K	0.00107	0.00069	0.00056	0.00057	0.00054		
64K	0.00092	0.00020	0.00014	0.00012	0.00012		64K	0.00007	0.00004	0.00004	0.00004	0.00004		64K	0.00067	0.00039	0.00036	0.00033	0.00033		
128K	0.00048	0.00012	0.00011	0.00011	0.00011		128K	0.00004	0.00004	0.00004	0.00004	0.00004		128K	0.00041	0.00036	0.00033	0.00033	0.00033		
256K	0.00039	0.00011	0.00011	0.00011	0.00011		256K	0.00004	0.00004	0.00004	0.00004	0.00004		256K	0.00037	0.00033	0.00033	0.00033	0.00033		
512K	0.00018	0.00011	0.00011	0.00011	0.00011		512K	0.00004	0.00004	0.00004	0.00004	0.00004		512K	0.00033	0.00033	0.00033	0.00033	0.00033		
1M	0.00012	0.00011	0.00011	0.00011	0.00011		1M	0.00004	0.00004	0.00004	0.00004	0.00004		1M	0.00033	0.00033	0.00033	0.00033	0.00033		
2M	0.00011	0.00011	0.00011	0.00011	0.00011		2M	0.00004	0.00004	0.00004	0.00004	0.00004		2M	0.00033	0.00033	0.00033	0.00033	0.00033		

Table 11: Average Miss Ratios for Berkeley Multimedia Workload (128 byte Block Size)

SPEC95

Table with 6 columns: Size, Direct, 2-way, 4-way, 8-way, 16-way. Sub-headers: SPEC95, Instruction Cache, Associativity, Data Cache, Unified Cache. Rows include sizes from 1K to 2M.

Block Size: 64 bytes

Table with 6 columns: Size, Direct, 2-way, 4-way, 8-way, 16-way. Sub-headers: SPECint95, Instruction Cache, Associativity, Data Cache, Unified Cache. Rows include sizes from 1K to 2M.

Table with 6 columns: Size, Direct, 2-way, 4-way, 8-way, 16-way. Sub-headers: SPECfp95, Instruction Cache, Associativity, Data Cache, Unified Cache. Rows include sizes from 1K to 2M.

SPEC95

Table with 6 columns: Size, Direct, 2-way, 4-way, 8-way, 16-way. Sub-headers: SPEC95, Instruction Cache, Associativity, Data Cache, Unified Cache. Rows include sizes from 1K to 2M.

Block Size: 128 bytes

Table with 6 columns: Size, Direct, 2-way, 4-way, 8-way, 16-way. Sub-headers: SPECint95, Instruction Cache, Associativity, Data Cache, Unified Cache. Rows include sizes from 1K to 2M.

Table with 6 columns: Size, Direct, 2-way, 4-way, 8-way, 16-way. Sub-headers: SPECfp95, Instruction Cache, Associativity, Data Cache, Unified Cache. Rows include sizes from 1K to 2M.

Table 14: Arithmetic Average Miss Ratio for SPEC95 (64, 128 byte Block Sizes)

SPEC95

SPEC95					
Instruction Cache					
Associativity					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.02236	0.02121			
2K	0.01619	0.01396	0.01396		
4K	0.01040	0.00914	0.00883	0.00893	
8K	0.00623	0.00533	0.00513	0.00507	0.00496
16K	0.00391	0.00288	0.00238	0.00225	0.00215
32K	0.00204	0.00124	0.00097	0.00097	0.00102
64K	0.00072	0.00037	0.00019	0.00014	0.00012
128K	0.00029	0.00007	0.00004	0.00003	0.00002
256K	0.00009	0.00002	0.00001	0.00001	0.00001
512K	0.00003	0.00001	0.00001	0.00001	0.00001
1M	0.00000	0.00000	0.00000	0.00000	0.00000
2M	0.00000	0.00000	0.00000	0.00000	0.00000
Data Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.41667	0.36569			
2K	0.30412	0.24760	0.21125		
4K	0.21680	0.16523	0.12738	0.10471	
8K	0.15203	0.11208	0.08499	0.06067	0.03559
16K	0.10690	0.07543	0.06130	0.04592	0.02279
32K	0.07109	0.04624	0.02767	0.02480	0.01341
64K	0.03799	0.02765	0.01280	0.01040	0.00947
128K	0.01758	0.01060	0.00993	0.00749	0.00753
256K	0.01057	0.00668	0.00654	0.00605	0.00611
512K	0.00633	0.00412	0.00338	0.00338	0.00341
1M	0.00363	0.00272	0.00257	0.00253	0.00254
2M	0.00260	0.00209	0.00206	0.00207	0.00208
Unified Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.28138	0.17229			
2K	0.19118	0.11599	0.10091		
4K	0.13093	0.07715	0.06237	0.05492	
8K	0.07943	0.05023	0.03877	0.03066	0.02233
16K	0.05024	0.03143	0.02595	0.02053	0.01248
32K	0.03393	0.01835	0.01186	0.01074	0.00680
64K	0.01741	0.01029	0.00511	0.00410	0.00368
128K	0.00795	0.00379	0.00331	0.00243	0.00242
256K	0.00454	0.00219	0.00207	0.00190	0.00191
512K	0.00244	0.00135	0.00109	0.00109	0.00110
1M	0.00169	0.00090	0.00084	0.00083	0.00083
2M	0.00130	0.00068	0.00067	0.00067	0.00068

Block Size: 256 bytes

SPECint95					
Instruction Cache					
Associativity					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.03692	0.03401			
2K	0.02813	0.02341	0.02265		
4K	0.01896	0.01640	0.01593	0.01610	
8K	0.01115	0.00957	0.00916	0.00895	0.00867
16K	0.00665	0.00503	0.00401	0.00373	0.00352
32K	0.00375	0.00224	0.00160	0.00124	0.00119
64K	0.00151	0.00079	0.00043	0.00031	0.00026
128K	0.00059	0.00016	0.00008	0.00006	0.00005
256K	0.00019	0.00004	0.00002	0.00002	0.00002
512K	0.00005	0.00001	0.00001	0.00001	0.00001
1M	0.00001	0.00000	0.00000	0.00000	0.00000
2M	0.00000	0.00000	0.00000	0.00000	0.00000
Data Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.35612	0.30264			
2K	0.25111	0.20744	0.17771		
4K	0.16943	0.12624	0.10715	0.09882	
8K	0.10831	0.07599	0.06561	0.05567	0.05192
16K	0.07119	0.04124	0.03438	0.03248	0.03064
32K	0.04689	0.02272	0.01806	0.01616	0.01562
64K	0.03068	0.01348	0.00987	0.00907	0.00881
128K	0.01603	0.00818	0.00676	0.00648	0.00644
256K	0.00899	0.00470	0.00437	0.00427	0.00426
512K	0.00465	0.00159	0.00152	0.00149	0.00147
1M	0.00061	0.00036	0.00032	0.00031	0.00031
2M	0.00037	0.00025	0.00023	0.00023	0.00023
Unified Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.26420	0.15450			
2K	0.18713	0.10727	0.09447		
4K	0.13043	0.07159	0.06196	0.05769	
8K	0.07065	0.04580	0.03806	0.03514	0.03401
16K	0.04156	0.02468	0.02112	0.01939	0.01851
32K	0.02763	0.01314	0.01030	0.00941	0.00900
64K	0.01455	0.00672	0.00474	0.00414	0.00384
128K	0.00730	0.00324	0.00232	0.00205	0.00198
256K	0.00325	0.00156	0.00130	0.00122	0.00121
512K	0.00145	0.00053	0.00045	0.00043	0.00041
1M	0.00055	0.00013	0.00011	0.00010	0.00010
2M	0.00041	0.00008	0.00007	0.00007	0.00007

SPECfp95					
Instruction Cache					
Associativity					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.01072	0.01097			
2K	0.00663	0.00639	0.00701		
4K	0.00356	0.00333	0.00315	0.00319	
8K	0.00229	0.00194	0.00190	0.00197	0.00200
16K	0.00171	0.00116	0.00107	0.00107	0.00105
32K	0.00068	0.00044	0.00047	0.00076	0.00089
64K	0.00009	0.00004	0.00000	0.00000	0.00000
128K	0.00005	0.00000	0.00000	0.00000	0.00000
256K	0.00001	0.00000	0.00000	0.00000	0.00000
512K	0.00001	0.00000	0.00000	0.00000	0.00000
1M	0.00000	0.00000	0.00000	0.00000	0.00000
2M	0.00000	0.00000	0.00000	0.00000	0.00000
Data Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.46511	0.41613			
2K	0.34652	0.27972	0.23807		
4K	0.25468	0.19641	0.14355	0.10942	
8K	0.18700	0.14094	0.10050	0.06468	0.02253
16K	0.13548	0.10278	0.08283	0.05667	0.01651
32K	0.09406	0.06506	0.03537	0.03172	0.01164
64K	0.04385	0.03898	0.01515	0.01146	0.01000
128K	0.01881	0.01254	0.01247	0.00829	0.00841
256K	0.01183	0.00826	0.00828	0.00748	0.00760
512K	0.00767	0.00615	0.00487	0.00490	0.00496
1M	0.00605	0.00461	0.00436	0.00431	0.00432
2M	0.00438	0.00356	0.00351	0.00354	0.00357
Unified Cache					
Size	Direct	2-way	4-way	8-way	16-way
1K	0.29513	0.18652			
2K	0.19442	0.12296	0.10607		
4K	0.13132	0.08159	0.06271	0.05270	
8K	0.08645	0.05377	0.03934	0.02708	0.01299
16K	0.05718	0.03683	0.02982	0.02145	0.00766
32K	0.03896	0.02252	0.01311	0.01181	0.00505
64K	0.01970	0.01314	0.00541	0.00407	0.00354
128K	0.00847	0.00423	0.00410	0.00274	0.00277
256K	0.00558	0.00269	0.00268	0.00244	0.00247
512K	0.00324	0.00201	0.00161	0.00162	0.00165
1M	0.00259	0.00151	0.00143	0.00141	0.00141
2M	0.00201	0.00117	0.00115	0.00116	0.00117

Table 15: Arithmetic Average Miss Ratios for SPEC95 (256 byte Block Size)